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(54) Multiple electrode field electron emission device and process for manufacturing it.

(57) Disclosed is a multiple electrode field electron emission device having a cathode (3) for emitting electrons by means of the field effect, a gate electrode (5) for establishing an electric field between said cathode and said gate electrode, an anode (7) for collecting the emitted electrons, and a control electrode (6) placed between said cathode (3) and said anode (7) for controlling the emitted electrons. Disclosed is also a method for manufacturing such a device in a manner to achieve emission projections (4) of the cathode (3) with a very small curvature radius and perfectly aligned to the gate electrode (5).

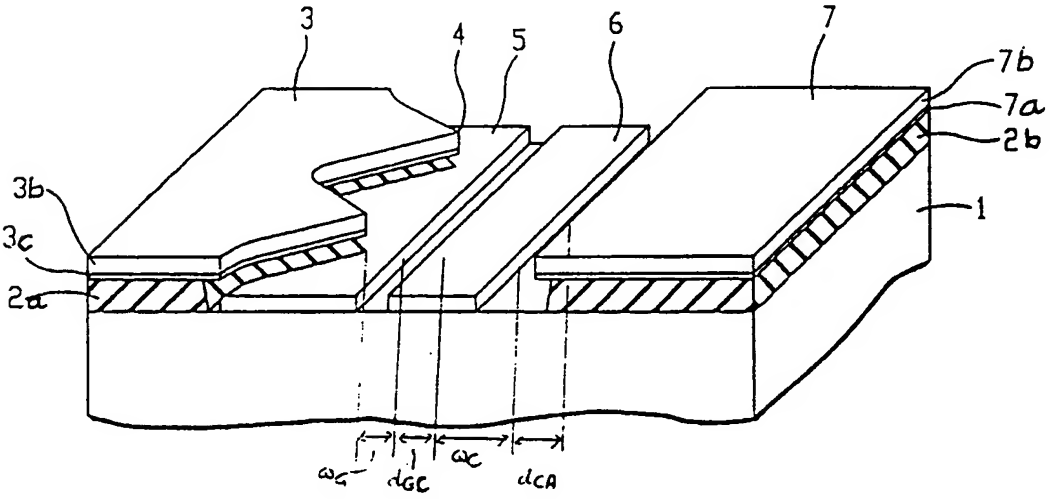

FIG.-1

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The present invention concerns a multiple electrode field lectron emission devic capable of controlling electrons that are field mitted from a cold cathode.

"Journal of Applied Physics", Vol. 59, No. 2, pages 164 to 169 (1990) disclos s a multiple electrode field electron mission devic as it is generally shown in Fig. 33. This device is called a flat triod device. It compris s on the surface of a quartz substrate base 101 an emitter electrode (cathode) 102 on one side, an anode 104 on the opposite side and a gate electrode 103 between the emitter electrode and the anode. The side of emitter electrode 102 facing the anode has a saw-tooth like structure, and the gate electrode 103 has column-shaped portions 103a. The three electrodes are formed by means of a photo-etching process from a tungsten thin film having a thickness of 1 μm. The teeth or projections of the emitter electrode 102 have a pitch of 10 μm and their number is 170. The distance between emitter electrode 102 and gate electrode 103 is 15 μm and the distance between gate electrode 103 and anode 104 is 10 μm.

When the electrical properties of this triode are measured in a vacuum of 5×10^{-6} Pa, the emitter emission current turns out to be a Fowler-Nordheim (F.N.) tunnel current. When the gate voltage is 220 V and the anode voltage 318 V, an anode current of about 1.2 μA is obtained. This amounts to about 7 nA of anode current for one tooth of the emitter electrode. The mutual conductance was about 0.1 μS.

This prior art triode device has a number of problems that will be discussed below. Electrons emitted from emitter electrode 102 proceed toward anode 104. However, because positively biased gate electrode 103 is located between the two electrodes, some of the emitted electrons will flow to this gate electrode. Because the gate current is equal to or higher than the anode current, the gate input resistance is very small. That is, the electron yield (anode current divided by total emission current) is small, causing a reduction in the electrical properties because characteristics such as the power efficiency and the mutual conductance are low. Using the technology of the prior art, the electron yield was at a level of 60%. For controlling the anode current of a triode device which has a low gate input resistance, it is necessary to have a driving circuit capable of handling large current and high power for applying the input signal to gate electrode 103. Because of this restriction it has been difficult to use these prior art triode devices as current amplifiers and power switches.

In addition, the emission current of the emitter is an F.N. tunnel current which increases and decreases exponentially relative to the gate voltage. As a result, the anode output current changes exponentially relative to the gate input signal. The triode device having such non-linear input to output relationship cannot be used for devices such as linear amplifiers.

Further, in order to enlarge the mutual conductance of the triode device and increase its performance, it is necessary to modify the structure of gate electrode 103 and enlarge the emission surface area of emitter electrode 102. However, if the emission surface area is enlarged, there will also be an increase in the amount of electrons that flow to gate electrode 103. Therefore, this prior art is not suitable for power amplifiers with high performance.

Cathode 102 and gate electrode 103 are fabricated in the same photo-etching process. The distance between these electrodes is determined by the resolution when photoresist exposure takes place. Practically, 0.8 μm is the lower limit of the resolution. Furthermore, as the process geometries become smaller, deviations increase. The threshold voltage of the electron emission of the field electron emission device and the uniformity of that voltage depend greatly on the distance between cathode 102 and gate electrode 103. As a result, it was difficult to reduce the threshold voltage of the triode devices of the prior art. Even if the threshold voltage was reduced, there would be the problem of poor uniformity.

The threshold voltage of the field electron emission device depends a great deal on the tip radius of curvature of the projecting teeth of cathode 102. That is, the smaller the tip curvature radius, the lower the threshold voltage. In order to obtain a practically usable threshold voltage, it is desirable to have a tip curvature radius of 100 nm or less. However, with the technology of the prior art, the lower limit is 200 nm because of the seepage of the photoresist. Fabrication of a practical tip radius of curvature was difficult.

It is an object of the present invention to overcome the problems of the prior art explained above and to provide a high performance multiple electrode field electron emission device having a large gate input resistance, a linear input to output relationship and a large mutual conductance. It is a further object of the invention to provide a process for manufacturing this multiple electrode field electron emission device.

These objects are achieved with a multiple electrode field electron emission device and a manufacturing process, respectively, as claimed.

With a device according to this invention, because the voltage of the control electrode and the anode current ar in a linear relationship, the input and output transfer characteristics are linear. Further, the anode resistance is very large. Therefore, the device is suitable for a linear amplifier.

With the invention, the ineffective current that flows to the gate l ctrode has been remarkably decreas d. From the perspective of current consumption, the invention provides a multiple electrode field electron emission device which has a good linear amplification effect.

Because the device according to this invention has a very large input resistance of the control electrode, it can be used in field effect amplifiers and switching devices.

Compared to thermal-electronic emission vacuum tubes of the prior art, the current, voltage and power that can be handled by a device according to the invention is either the same or better. Furthermore, the device according to the invention is very small.

Because the mutual conductance and the degree of linearity of the transfer characteristics can be controlled by the gate voltage, even using the same device, special parameters can easily form different circuits.

The invention further allows for a great degree of freedom in configuring a device that fits the needs of a particular application, such as a device with excellent frequency characteristics, a device with excellent power efficiency or a device that is able to handle high and low power supply voltages.

Preferred embodiments of the invention will be described below with reference to the schematic drawings, in which:

Fig. 1 is an angular view of a tetrode field electron emission device according to a first embodiment of the invention,

Figs. 2(A) through (F) are sectional views illustrating various process steps of a process for manufacturing the device of Fig. 1,

Fig. 3 is an angular view of a triode field electron emission device used for explaining a second embodiment of this invention,

Figs. 4(A) through (F) are sectional views illustrating various process steps of a process for manufacturing the device of Fig. 3,

Figs. 5(A) through (C) are plan views corresponding to Figs. 4(B), (D) and (E), respectively,

Figs. 6(A) and (B) show a plan view and a sectional view, respectively, of a flat tetrode vacuum tube using the tetrode field electron emission device of Fig. 1,

Fig. 7 is a circuit diagram using a tetrode field electron emission device in a cathode grounded configuration,

Fig. 8 is a graph illustrating the electron emission characteristics obtained with the circuit diagram of Fig. 7,

Fig. 9 is a graph illustrating the input and output electrostatic characteristics obtained with the circuit diagram of Fig. 7,

Fig. 10 is a graph illustrating the anode electrostatic characteristics obtained with the circuit diagram of Fig. 7,

Fig. 11 shows the relationship between gate current, anode current, control current and control voltage of the tetrode field electron emission device,

Fig. 12 shows the anode characteristics of the tetrode field electron emission device,

Fig. 13 is another circuit diagram using the tetrode field electron emission device in a gate grounded configuration,

Fig. 14 is another circuit diagram of a tetrode field electron emission device,

Fig. 15 shows the anode characteristics obtained with the circuit diagram of Fig. 14,

Fig. 16 is a circuit diagram of a pentode field electron emission device,

Fig. 17 shows the anode characteristics obtained with the circuit diagram of Fig. 16,

Figs. 18(A), (B) and (C) are a plan view and cross-sectional views, respectively, of a hexode field electron emission device according to a third embodiment of the invention,

Figs. 19(A) through (G) are sectional views illustrating various process steps of a process for manufacturing the hexode field electron emission device of Fig. 18,

Fig. 20 is an angular view of a hexode vacuum tube using the hexode field electron emission device,

Fig. 21 is a circuit diagram of the hexode field electron emission device,

Fig. 22 shows another circuit diagram of the hexode field electron emission device,

Fig. 23 is illustrates the anode characteristics obtained with the circuit diagram of Fig. 22,

Fig. 24 is a cross-sectional view of a vertical tetrode field electron emission device according to a fourth embodiment of the invention,

Fig. 25 is an angular view of a tetrode field electron emission device of a modified embodiment of the invention where openings are provided in the gate electrode and the control electrode,

Fig. 26 is an angular view of a modified embodiment of the invention differing from that of Fig. 25 by using a control electrode with column-shaped electrode portions,

Fig. 27(a) shows a triode field electron emission device according to a fifth embodiment of this invention,

Fig. 27(b) is a sectional view along line a-a of Fig. 27(a),

Fig. 27(c) is a cross-sectional view along line b-b of Fig. 27(a),

Fig. 27(d) is an angular view of a part of the device of Fig. 27(a),

Figs. 28(a) through (c), Figs. 29(a) through (d) and

Figs. 30(a) and (b) illustrate various process steps of the process for manufacturing the triod field electron mission devic of Fig. 27.

Fig. 31 illustrates th formation of a bridge in the manufacturing process according to Figs. 29 t 30,

Figs. 32(a) through (g) illustrat a modification of the manufacturing process according to Figs. 29 to 30, and

Fig. 33 shows a triode field electron emission device according to the prior art.

With reference to Figs. 1 and 2(A) to (F) a first embodiment of the invention will be described.

Fig. 1 is a perspective view showing the structure of a tetrode field electron emission device. This device comprises on the surface of a flat substrate base 1 made of quartz, a gate electrode 5 and a control electrode 6 which are made of a molybdenum (Mo) thin film having a thickness of 100 nm. The gate electrode 5 and the control electrode 6 are arranged between 2 separate, island shaped portions 2a and 2b of an insulating layer having a thickness of 500 nm and being made of silicon dioxide. On the surface of insulating layer portion 2a which is adjacent to gate electrode 5, there is a cathode 3 which has a thickness of 200 nm. The side of the cathode 3 facing the gate electrode 5 has a saw-tooth like shape, the teeth forming overhanging emission projections 4, i.e. the emission projections extend in parallel to the surface of substrate base 1 beyond the edge of underlying insulating layer portion 2a. On the surface of the insulating layer portion 2b which is adjacent to control electrode 6, there is an anode 7 which has a thickness of 200 nm.

Cathode 3 comprises two layers, namely a deposited first or lower cathode layer 3a, having a film thickness of 100 nm and being made of tungsten (W) and a deposited second or upper cathode layer 3b having a film thickness of 100 nm and being made of molybdenum (Mo). Like cathode 3, anode 7 comprises a first anode layer 7a and a second anode layer 7b, both deposited. The four electrodes, that is cathode 3, gate electrode 5, control electrode 6 and anode 7 are disposed on the surface of base 1 in a lengthwise direction in this sequence.

Emission projections 4 of cathode 3 are arranged at a pitch of 5 μm and project towards the side of gate electrode 5. Insulating layer portion 2a is shaped such that it does not exist in the vicinity of the emission projection tips. The tip curvature radius of the emission projections 4 within the plane parallel to the flat surface of base 1 is about 40 nm.

Gate electrode 5 is formed self-aligned to cathode 3 and is provided with recessions of a shape substantially corresponding to the projection of the respective emission projection 4 onto the plane of gate electrode 5, i.e. the edge of gate electrode 5 facing the cathode side has a saw-tooth like shape substantially complementary to that of cathode 3. The distance (L_{GK}) between gate electrode 5 and emission projections 4 in the direction perpendicular to the surface of base 1 is determined by the film thicknesses of insulating layer portion 2a and gate electrode layer 5, that is the distance equals the difference between those film thicknesses. A suitable value for the distance L_{GK} is 400 nm. With the recent methods of structuring thin films the film thickness can be accurately controlled. As a result, the controllability, reproducibility and uniformity of the distance L_{GK} is excellent.

The width w_G of the gate electrode 5 in the vicinity of the tips of emission projections 4 is about 2 μm (measured along a horizontal line in Fig. 1). The distance (space) d_{GC} between gate electrode 5 and control electrode 6 is 4 μm. The width w_C of control electrode 6 is 8 μm (measured along a horizontal line in Fig. 1). The distance (space) d_{GA} between control electrode 6 and anode 7 is about 10 μm. The smaller the width of gate electrode 5, the smaller the gate current and the better the power efficiency. Also, the larger the width and surface area of anode 7, the better the electron yield. The wider the width of control electrode 6, the larger the mutual conductance and the greater the controllability of the anode current. However, because the amount of electrons (control current) that flow to the control electrode 6 increases as the width of control electrode 6 increases, the width of the control electrode is determined on the basis of a trade-off between these factors. It is ideal to have the dimensions in a range in which the width of control electrode 6 is greater than the width of gate electrode 5 but smaller than that of anode 7. To increase the amplification factor μ ($= C_{CG}/C_{AG}$, C_{CG} is the capacity between gate electrode 5 and control electrode 6 and C_{AG} is the capacity between gate electrode 5 and anode 7) means to decrease the width of control electrode 6 and to enlarge the space between control electrode 6 and anode 7.

The fabrication process of the tetrode field electron emission device shown in Fig. 1 will now be explained with reference to Fig. 2. Figs. 2(A) to (F) are vertical cross-sectional views showing the device at the end of respective process steps.

Fig. 2(A) shows the device after an insulating layer 8, a cathode layer 9 and an etching passivation layer 10 have been deposited in this sequence on the surface of flat substrate bas 1 and aft r a photoresist lay r 11 has been formed and patt rned on etching passivation layer 10. Flat substrat bas 1 is an insulating quartz substrate. Insulating layer 8, cathode layer 9 and etching passivation layer 10 are deposited one after the other by sputtering. Insulating layer 8, cathode layer 9 and etching passivation layer 10 are composed of a 500 nm

silicon dioxid thin film, a 100 nm tungsten thin film and a 200 nm silicon dioxid thin film, respectively. Photoresist layer 11 has been patterned corresponding to the desired shapes of cathod 3 and anode 7.

Figure 2(B) shows th device in a state when an etching mask 12 has been formed by exc ss- tching of etching passivation layer 10. This excess-etching method us s an tching means that sel ctiv ly etches etching passivation layer 10 using an HF-type etching solution so that even more of etching passivation layer 10 is etched away than is determined by the shape of photoresist layer 11. It is possible to form etching mask 12 with a small radius of curvature of its portions corresponding to emission projections 4, by excess-etching passivation layer 10 from the outer periphery inwardly beneath photoresist layer 11. In this embodiment, the curvature radius of the portions of the photoresist layer 11 corresponding to the tip portions of emission projections 4 was 300 nm. With an excess-etching of 500 nm an etching mask 12 having a tip curvature radius of only 30 nm was obtained.

Fig. 2(C) shows the device in a state when cathode layer 9 has been etched to form first cathode layer 3a and first anode layer 7a. Etching mask 12 which has sharp projections corresponding to the emission projections is used in processing cathode layer 9 after removal of photoresist layer 11. Cathode layer 9 is processed by dry etching for 5 minutes at a gas flow ratio of CF_4/O_2=60/200 and an RF power of 700 W. At this time, cathode layer 9 is excess-etched to obtain first cathode layer 3a, which has sharp emission projections with a tip curvature radius of 30 nm.

Fig. 2(D) shows the device in a state when insulating layer 8 has been partially etched away forming island shaped insulating layer portions 2a and 2b and exposing emission projections 4a. The first cathode layer 3a and the first anode layer 7a are used as etching masks to remove the unnecessary portion of insulating layer 8 with an HF etching solution. At this time, the emission projections 4a are exposed such that they overhang from insulating layer portion 2a. Also, etching mask 12 is removed and the flat substrate base 1 shows almost no etching because it is made of quartz.

Fig. 2(E) shows the device in a state, when a gate electrode layer 13 has been formed by using a directional particulate deposition method. Sputtering is used as the directional particulate deposition method to deposit a molybdenum (Mo) thin film layer of 100 nm thickness as the gate electrode layer 13. With the directional particulate deposition method, particles are shot out from a particle source in a direction nearly normal to the surface of flat substrate base 1 and deposited on this surface. When this method is used, the overhanging portions, such as emission projections 4a, form a cover so that a molybdenum thin film layer 131 is deposited on top of the first cathode layer 3a, a molybdenum thin film layer 132 is deposited on the surface of the first anode layer 7a and the gate electrode layer 13 is deposited on the surface of the flat substrate base 1 in a way that all of these tree layers are electrically isolated from each other. It goes without saying that by this technique emission projections 4b of thin film layer 131 and recessions in gate electrode layer 13, which have the same shape as the emission projections 4a are formed self-aligned to the emission projections 4a. Vapor deposition, sputtering, electron cyclotron resonance (ECR), plasma deposition and the clustered ion beam can be used as the directional particulate deposition method.

Fig. 2(F) shows the device in a state when gate electrode layer 13 and thin film layers 131 and 132 have been etched to form gate electrode 5, control electrode 6, the second cathode layer 3b and the second anode layer 7b. A photo-etching technology is used and after a photoresist has been applied in a pattern corresponding to the second cathode layer 3b, the gate electrode 5, the control electrode 6 and the second anode layer 7b, the molybdenum thin film is etched using dry etching.

The tip curvature radius of the emission projections 4 of cathode 3 of a completed multiple electrode field electron emission device is 40 nm. This is due to an increased roundness of the first cathode layer 3a because of the deposition of the second cathode layer 3b. However, this roundness causes the surface area of emission projections 4 that is in the electric field to enlarge, making it possible to obtain electron emissions that are large in volume and stable. In a case, in which the materials used for the first cathode layer 3a and the second cathode layer 3b are different, for the most part, if either the emission projections 4a of the first cathode layer 3a or the emission projections 4b of the second cathode layer 3b are etched away, the resulting emission projections 4 will become thinner and the film thickness direction tip curvature radius will become smaller resulting in a multiple electrode field electron emission device that has a low threshold value.

It is possible to fabricate a multiple field electron emission device with emission projections having a very small tip curvature radius by a manufacturing method using an etching mask formed by excess-etching of the insulating layer instead of using etching mask 12 made from etching passivation layer 10 as mentioned above. A corresponding manufacturing method will be described below, using a triode field electron emission device as an xample.

Fig. 3 is an angular view of the triode field electron emission device manufactur d by such manufacturing process.

The major components of this device are a flat substrate base 1, an island-shaped insulating layer 202, a

cathode 203 quipp d with saw-tooth like emission proj ctions 4 form d as overhanging portions of the cathode 203, a gate electrode 205 and an anode 7. The gate l ctrode 205 is formed s lf-align d to the emission projections 4 and the anode 7 is formed on the surface of flat substrate base 1. The island shaped insulating layer 202 is formed on an el vated portion of the substrate surface and a sloped surface portion 213 around the island-shaped insulating layer 202, particularly in the vicinity of gate electrode 205, connects the elevated surface portion to the rest of the substrate surface. Sloped surface portion 213 has the advantage of reducing the flow of electrons emitted from emission projections 4 to gate electrode 5, thereby improving the power efficiency of the field electron emission device.

In this case, the field electron emission device has 100 emission projections 4, that are aligned in a row at a pitch of 5 μm. The tip curvature radius of the emission projections 4 is 40 nm. The distance between cathode 203 and gate electrode 205 (L_{GK}) is 400 nm. The width of gate electrode 205 at the tips of the emission projections 4 is 2 μm. The distance between cathode 203 and anode 7 (L_{AK}) is about 10 μm. Flat substrate base 1 is a glass substrate (#7059 glass substrate made by Corning). Island-shaped insulating layer 202 is made of a 500 nm thick silicon oxide film. Cathode 203 comprises a first or lower cathode layer 203a made of a 100 nm thick molybdenum (Mo) thin film and a second or upper cathode layer 203b. The upper cathode layer 203b, the gate electrode 205 and the anode 7 are all made of a 200 nm thick tantalum (Ta) thin film. The slope angle of sloped surface portion 213 is about 10°.

Figs. 4(A) to (F) are cross-sectional views illustrating various steps of the process for manufacturing the field electron emission device shown in Fig. 3. Figs. 5(A) through (C) are plan views corresponding to Figs. 4(B), (D) and (E), respectively.

First of all, an insulating layer 8 and a cathode layer 9 are formed on the surface of flat substrate base 1. After that a resist layer 11 is formed (Fig. 4(A)). Flat substrate base 1 is a glass substrate as mentioned before that has insulating properties. Insulating layer 8 is a 500 nm dioxide thin film formed by atmospheric pressure CVD. Cathode layer 9 is a 100 nm molybdenum (Mo) thin film layer, deposited by sputtering. Resist layer 11 is generally in the shape of cathode 203 and is formed using photo-etching.

Next, the cathode layer 9 is processed to the shape of resist layer 11 to form temporary cathode layer 91 (Fig. 4(B) and Fig. 5(A)). To that end the cathode layer 9 is etched by means of a dry etching method using CF_4 gas. The tips 11a of saw-tooth like projections of the resist layer 11 have a tip curvature radius of 700 nm and the tips of corresponding projections of temporary cathode layer 91 have the same tip curvature radius.

In the next step an etching mask 81 is formed by excess-etching of insulating layer 8 (Fig. 4(C)). Excess-etching is a method by which insulating layer 8 is etched away deep within a stipulated region in temporary cathode layer 91 using an isotropic etching means. Because etching of insulating layer 8 progresses at an equal rate from the outer periphery in an inward direction when isotropic etching is used, the convex areas have a sharp shape, i.e. excess-etching results in a small tip curvature radius in the convex areas of etching mask 81.

An HF type etching solution is used as the isotropic etching means to excess-etch the silicon dioxide thin film forming insulating layer 8. When it is etched to 1.5 μm inward from the outer periphery of temporary cathode layer 91, reverse taper-shaped etching mask 81 is formed with protruding portions having a tip curvature radius of 30 nm. Compared to the 700 nm tip curvature radius of temporary cathode layer 91, a twenty-fold increase in sharpness is achieved. In this process, the surface of flat substrate base 1 is etched to form sloped surface portion 213 around etching mask 81. The etching speed of the insulating layer 8 is five times faster than that of substrate base 1. As a result, the slope of the surface portion 213 that is formed beneath the emission projections 4 is about 10°.

Next, temporary cathode layer 91 is etched to the shape of etching mask 81 to form first cathode layer 203a (Fig. 4(D) and Fig. 5(B)). With resist layer 11 covering the upper surface of temporary cathode layer 91 for protection, when etched from lower side, first cathode layer 203a is formed to have the same shape as the side of the etching mask 81 contacting it. The tip curvature radius of emission projections 4a of the first cathode layer 203a is about 30 nm.

Next, the sides of etching mask 81 are etched away to form island-shaped insulating layer 202, and resist layer 11 is removed (Fig. 4(E) and Fig. 5(C)). 0,7 μm of the sides of etching mask 81 are removed so that the first cathode layer 203a gets the shape of an eaves with overhanging and exposed emission projections 4a.

Finally, after forming a Ta thin film electrode layer at a thickness of 200 nm using directional particulate deposition, this layer is etched to obtain the second cathode layer 203b, gate electrode 205 and anode 7 (Fig. 4(F)). Sputtering is used for this directional particulate deposition. With this deposition, the overhanging portions, such as emission projections 4a, act as a cover, and the second cathode layer 203b, which is deposited on the surface of the first cathod lay r 203a and th rest of the electrode layer deposit d on th surfac of flat substrate base 1 become lectrically isolated from each other.

Portions of the second cathod layer 203b deposit d on emission projections 4a of th first cathode lay r 203a become emission projections 4b, and emission projections 4a and 4b form together the emission projec-

tions 4. Gate electrode 205 is formed with recessions corresponding in shape and being self-aligned to emission projections 4a. Sputt ring, vapor deposition, ECR (lectron cyclotron resonanc), plasma deposition and the cluster ion beam method are some of the methods that can be used as dir ctional particulate depositi n methods. The Ta thin film l ctrod layer is process d by m ans of dry etching to form th gate lectrode 205 and anode 7. At this time, it is important to cover the layer with a photoresist so that the recessions corresponding to emission projections 4 are not corroded. The first and lower cathode layer 203a and the second and upper cathode layer 203b form together cathode 203. The tip curvature radius of the emission projections 4 is about 40 nm. In a case in which different materials are used for the first and second cathode layers 203a and 203b, one of the two layers may be removed at the emission projections and only the remainder used as electron emission electrode. If the emission projections are made thin in this manner, the tip curvature radius in the direction of the film thickness will become smaller, allowing lower threshold voltages to be achieved.

A field electron emission device manufactured in this manner was measured in high vacuum. When cathode 203 was grounded and the voltage between anode and cathode was constant at V_{AK} = 200 V, at a voltage of V_{GK} = 60 V between gate and cathode, the cathode current was $I_K = 4 \times 10^{-8}$ A. At V_{GK} = 100 V a cathode current of 6×10^{-5} A was obtained. The parasitic capacitance between cathode 203 and gate electrode 205 was 10 fF.

In this embodiment, the materials used for the electrodes, such as for cathode 203, were molybdenum and tantalum thin films. However, this invention is not limited to these materials. Instead, other materials that can be used are metals such as tungsten, silicon, chrome and aluminum and alloys that contain these metals. Furthermore, as flat substrate base 1, substrates such as ceramics substrates with good thermal conductance can be used. For instance, an insulating substrate base like an alumina substrate base or an insulator on the surface of a conductive substrate base, such as a silicon substrate base, may be used. Moreover, insulating layer 8 and etching mask 81 are not limited to a silicon dioxide thin film. Thin films such as silicon nitride thin films and alumina thin films may also be used.

In order to reduce the threshold voltage of the electron emission it is feasible to coat emission projections 4 with materials that have a small work function, such as barium, thorium and cesium. In addition, cathode 203 may be made of such a material.

In order to reduce the noise from electron emissions, it is possible to create an adequate number of emission projections 4 and to increase the S/N ratio by driving these emission projections and creating electron emissions at the same time. Electron emissions do not have to originate at one point, that is the tip of the emission projections. They can originate from auxiliary projections created on the side of the tip, and this will provide the same effect. In addition, excessive current flow and noise can be prevented by connecting a self-bias resistor or non-linear resistor directly to the cathode.

By putting a fluorescent material on the surface of anode 7, a light emitting display may be formed. By using a material such as a copper thin film that generates X-rays and exciting this with an electron beam, it is possible to create a minute X-ray source.

For reasons of simplification the above manufacturing process has been described with reference to a triode field electron emission device since the main difference between this process and that of Figs. 2(A) to (F) is the way of fabricating the cathode. It will be appreciated that the process of Figs. 4(A) to (F) can be easily modified to manufacture a multiple electrode field electron emission device according to the invention, namely a tetrode, pentode, etc. The process steps for manufacturing the cathode and the gate will remain unchanged.

As described above, the manufacturing process of the field electron emission device of this invention has the following effects:

(1) Compared to fabricating the cathode by excess-etching the cathode layer itself, by excess-etching the etching mask layer formed on the surface of the substrate base, it is possible to fabricate emission projections with a smaller tip curvature radius. This is because the etching properties of the etching mask formed on the surface of flat substrate base 1 are very isotropic and because etching methods that etch at a fast rate, such as wet etching, can be used. Because it is difficult to apply wet etching to materials such as molybdenum, it is also difficult to form emission projections 4 by means of excess-etching such materials.

(2) L_{GK} is generally determined by the film thickness of the island-shaped insulating layer and that of the gate electrode. The ability to control the film thickness has become excellent as LSI process technology has progressed, making it possible to achieve a field electron emission device with excellent uniformity and a low electron emission threshold voltage. With the technology of the prior art, the lower limit of L_{GK} was 0.8 μm. However, as a result of this invention, it is possible to fabricate and obtain a value for L_{GK} of 0.1 μm or lower.

(3) Emission projections with a small tip curvatur radius and a low threshold voltag are achiev d by using excess-etching. With the t chnology of th prior art, the lower limit of th tip curvatur radius is 200 nm. With this invention it is possibl to obtain a curvature radius of 40 nm or l ss.

(4) The advantage of using excess-etching is, that convex areas, such as mission projections 4 hav a smaller, sharper tip curvature radius. Conv rsely, the concave areas ar much smoother. Such convex and concav areas of the cathode allow to pr v nt accidental electron missions and shortening between th el ctrodes.

(5) As explained above, the invention allows to create a gate electrode self-aligned to the cathode which results in a reduction of the parasitic capacitance between the electrodes and, thus, a high-speed operation. In particular, providing the first cathode layer with a low resistivity is suitable for high-speed devices with a low line resistance and smaller line delays.

Fig. 6(A) schematically shows a plan view of a flat tetrode vacuum tube that uses the new tetrode field electron emission device described above. Fig. 6(B) is a cross sectional view along line A-A in Fig. 6(A). The flat tetrode vacuum tube comprises the flat substrate base 1 with the above described tetrode field electron emission device thereon, and an opposing substrate base 14. The substrate bases are disposed nearly parallel to each other with a support 17 therebetween extending around the periphery. The tetrode field electron emission device is sealed within a space 23 which is surrounded by substrate base 1, opposing substrate base 14 and support 17. The space 23 is evacuated. Substrate base 14 is a quartz substrate having a conductive thin film 15 on its inner surface to prevent electrostatic charges. A port 16 in the substrate base 14 is used for evacuation and after evacuation sealed by melting an Au and Sn alloy inside of the port which is covered with a Cr/Au thin film. A getter material 18 made of an Al and Ba thin film alloy is formed in advance on the inner surface of opposing substrate base 14. After evacuation of space 23 has been completed, this getter material is heated by a laser, thereby evaporated and deposited on the walls of space 23 to activate the gettering effect.

Support 17 is a baked mixture of low melting point glass powder and glass fibres with a diameter of 100 μm. It seals and adheres well to each substrate base and maintains the height of space 23 (gap) at 100 μm.

The external pins of the tetrode field electron emission device, that is, cathode pin 19, gate pin 20, control pin 21 and anode pin 22, are formed from metal thin films and extend to the outside of vacuum space 23 between flat substrate base 1 and support 17. The size of this flat tetrode vacuum tube is 7 mm length, 4 mm width and 2.2 mm thickness. Compared to the thermo-electronic emission type vacuum tubes of the prior art this is very small, namely a volume of 1/1000 or less of that of the prior art vacuum tubes. The degree of vacuum In vacuum space 23 is 133×10^{-7} Pa (1×10^{-7} Torr) or less. In this example anode 7 is formed on the surface of flat substrate base 1. However, this invention is not limited to that. For example, the anode may be formed on the surface of the opposing substrate base 14. Also, in this case, control electrode 6 may be placed within vacuum space 23 so that it is located between emission projections 4 and anode 7.

Figs. 7 through 9 show the electrical properties of the tetrode field electron emission device described above. Fig. 7 is a circuit diagram of a cathode grounded voltage amplifier using such tetrode field emission device. The tetrode vacuum tube described above is represented by symbol mark 30 which is shown in the center of Fig. 7. This indicates that cathode 3, gate 5, control electrode 6 and anode 7 have been sealed inside of vacuum space 23.

The method of driving a voltage amplifier that uses a tetrode field electron emission device is as follows: Cathode 3 is grounded and a positive bias gate voltage V_{GK} is applied between gate 5 and ground by means of a voltage source 26. A voltage source 27 is connected between anode 7 via a load resistor 28 and ground to apply a positive anode voltage V_{Ak} to anode 7. A voltage source 25 providing a control bias voltage V_{CK} and an input signal voltage source 24 are connected in series between control electrode 6 and ground. An output signal voltage V_o which is proportional to the input signal voltage V_I of voltage source 24 is obtained at terminal 29 from anode 7 and load resistor 28.

Fig. 8 is a graph showing the electron emission properties of the aforesaid tetrode field electron emission device, namely the gate current versus gate voltage (I_G-V_{GK}) and the anode current versus gate voltage (I_A-V_{GK}) characteristics. In this case the input signal voltage V_I of voltage source 24 and the control bias voltage V_{CK} of voltage source 25 in the circuit diagram of Fig. 7 were set to 0 V. Gate current I_G and anode current I_A increase exponentially relative to gate voltage V_{GK} indicating that the emission current is the F.N. tunnel current. The anode current is about 2 digits smaller than the gate current. In the driving method of the prior art, which controls the anode current by the gate voltage, the electric power conversion efficiency was poor because $I_G > I_A$. In addition, because the transfer characteristics are also exponentional, it is difficult to use this method in a linear amplifier. For this reason, the anode current I_A is controlled by the voltage applied to control electrode 6.

Fig. 9 is a graph showing the input and output static characteristics of the aforesaid tetrode field electrode emission devic , namely the control current versus control bias voltag (I_C-V_{CK}) and the anode current versus control bias voltage (I_A-V_{CK}) characteristics. In this case the gat voltage was $V_{GK} = 140$ V, the input signal voltage $V_I = 0$ V and the anode voltag $V_{AK} = 400$ V in the circuit diagram of Fig. 7. Although the anod current changes exponentially (non-linearly) in the range of $V_{CK} < 0$, the anode curr nt characteristic is a straight line

(linear characteristic) in the rang of $V_{CK} > 0$. That is, in th rang of $V_{CK} > 0$, anode current I_A is proportional to th voltage applied to control el ctr de 6. Therefore the tetrod field el ctron emission d vice according to the invention can be used as a linear amplifier. At this time, the control current I_C is 1% or less of th an de current I_A, yi lding a field effect voltage amplifier with excellent input and output power conversion efficiency.

The anode current control mechanism by the field effect of control electrode 6 is similar to the control by the grid electrode of a prior art thermo-electronic emission vacuum tube. That is, it is a mechanism in which the anode current is controlled by the electric field (bias gradient) formed between control electrode 6 and cathode 3 by means of the bias of control electrode 6. If a negative voltage is applied to control electrode 6 and a negative electric field is formed in the vicinity of emission projections 4, a repelling force will be applied to the emitted electrons going toward anode 7, and the number of electrons that reach anode 7 will be limited.

Since the electrons emitted from the cathode will have an initial speed, they will travel in the direction of the anode. However, if a control electrode exists inbetween with a negative bias, their speed will be reduced by the bias gradient of the negative bias and some of the electrons will return to the cathode. In this manner, electrons will remain between the cathode and the control electrode and form an electron cloud (space charge limited area). Electrons that are able to flow toward the anode are statistically limited to those whose energy is higher than the control bias. It is known that the transfer of electrons in such a space charge limited area yields noise current that is very small. The fluctuation of the space charge is small compared to the emission current fluctuation (noise current) from the cathode. In particular, the fluctuation of electrons having a small amount of energy can be ignored. Only some of the electrons, those with a lot if energy, become cause for the noise of the anode current. The triode field electron emission device of the prior art does not have the space charge control area described above. Most of the electrons that are emitted from the cathode reach the anode (transfer of electrons in the emission limited area). Therefore, the emission current noise is expressed as the anode current noise.

However, if positive voltage is applied to control electrode 6, the strength of the repulsive force on the emitted electrons will be weaker and the anode current will increase. By the way, positive bias gate electrode 5 performs the same role as the space charge grid electrode of a prior art pentode vacuum tube and prevents the retention of space charge in the area of cathode 3. As will be discussed later, according to this invention, a further control electrode may be added between anode 7 and control electrode 6 to prevent the effects of secondary electrons from anode 7.

The linear and non-linear areas of the characteristics can be properly utilized by suitably setting the control bias voltage V_{CK}. The linear area is suitable for a linear amplification function such as in a voltage amplifier. The non-linear area is suitable for functions such as switching. Also, if gate voltage V_{GK} is lowered, the control bias voltage at which the transition between the linear area and the non-linear area occurs, will shift to the low voltage side. Therefore, the control bias voltage V_{CK} may be freely selected by suitably setting gate voltage V_{GK}.

However, as shown in Fig. 8, in the tetrode field electron emission device described above, the gate current I_G is significantly higher than the anode current I_A, and the parasitic current that flows to the gate electrode is inefficient.

Fig. 10 is a graph showing the anode static characteristics of the multiple electrode field electron emission device of this embodiment. Shown are the I_A-V_{AK} static characteristics for a gate voltage V_{GK} = 140 V, an input signal voltage V_I = 0 V and control bias voltages V_{CK} = 20 V, 40 V, 60 V and 80 V, respectively, in the circuit diagram of Fig. 7. As will be understood from Fig. 10, in the multiple electrode field emission device of this embodiment, I_A becomes almost constant in the range of $V_{AK} > 150$ V. Also, I_A increases in proportion to V_{GK}, which is an anode static characteristic that is similar to the thermo-electronic emission pentode vacuum tube of the prior art. This characteristic is suitable for linear amplifier applications etc. because the anode resistance if very large and the input and output are in a proportional relationship.

If load resistor 28 in Fig. 7 has a value of R_L = 5 GΩ, load line 36 can be drawn in the graph of Fig. 10. The basic functions have been confirmed as those of an amplifier by the means of such a circuit. That is, when control bias voltage was V_{CK} = 40 V and a 20 V sine wave ($V_I = 20 \sin(\omega t)$ V) was applied as input signal by input signal source 24, a 50 V sine wave ($V_o = -50 \sin(\omega t)$ V) was obtained as the output signal at terminal 29. Thus, the amplification ratio was 2.5. When the amplifier characteristics were measured while increasing the frequency ω, the cutoff frequency ω_c was 100 MHz or more. Fig. 11 shows the relationship between the control voltage V_{CK} and the gate current I_G, the anode current I_A and the control current I_C, respectively. For $V_{CK} < V_{GK}$ the control current I_C is negative. An ion current in the vacuum and a leak current on the surface of the substrate base are possible reasons for this negativ current. However, becaus th current is stable, it is probably a surfac leak curr nt betwe n th gates. Anod current I_A increases monotonally in relation t th control v ltag V_{CK}. When the control voltage is especially larg , the anode current will increase almost proportionally with an increase of the control voltage. That is, a linear region has been found for the transfer characteristics. It has been dis-

covered that the emission current is nearly constant relative to V_{CK} and is determined by the gate voltage and not influenced by the bias of other electrodes.

Fig. 12 shows the anode characteristics (I_A - V_{AK}) with the control voltage V_{CK} as parameter (it should be understood that the difference between Fig. 10 and Fig. 12 is due to the fact that Fig. 10 is based on presumed data while Fig. 12 is based on experimental data). Anode current I_A increases with an increase of both, anode voltage V_{AK} and control voltage V_{CK} in accordance with the following equation:

$$I_A = K(V_{CK} + aV_{AK})^n$$

Here, K, a and n are constants. The characteristics are the same as those for a thermo-electronic emission triode vacuum tube in a space charge limited area. By estimating the amplification rate μ (= 1/a) and the mutual conductance Gm (= dI_A/dV_{CK}) from this diagram for V_{AK} = 330 V and V_{CK} = 150 V, they are 1 and 2.6 E-10 S, respectively. The value n was about 1.3. When $V_{CK} > V_{GK}$, there is a tendency for some of the anode current to flow to the control electrode.

In the characteristics shown in Fig. 12, the values of Gm and μ are very small. Practically, values of 1 mS or more and 100 or more, respectively, are demanded. There are a number of ways of improving both. However, the in the case of Gm, in particular, it is effective to increase the emission current.

In order to further increase the voltage amplification rate, increase the mutual conductance and improve the frequency characteristic, it is necessary to either increase the number of emission projections of cathode 3 or devise a structure for the gate electrode 5 that reduces the ineffective gate current and increases the anode current. In this embodiment, there are six emission projections 4. However, if, for example, this number was increased 10,000 times and the emission current was increased 10,000 fold, the voltage amplification rate and the mutual conductance would increase approximately 10,000 fold, allowing the frequency characteristic to improve about 100 times. To decrease the amount of ineffective gate current, the probability of emitted electrons impacting with gate electrode 5 could be reduced by structuring the gate electrode so that it has a smaller width, or giving it a structure such that it is on an inclined plane as in Fig. 3 with an open angle in the direction in which emission projections 4 project outward.

In this embodiment, cathode 3 was grounded. However, this invention is not limited to that. For example, gate electrode 5 could be grounded instead. Fig. 13 is a circuit diagram using the multiple electrode field electron emission device of this embodiment in a voltage amplifier in which the gate electrode is grounded and a negative voltage V_{KG} of a cathode voltage source 37 is applied to cathode 3. This circuit diagram is different from that of Fig. 7 and the amplifier it shows is easy to use because the border line between the linear area and the non-linear area does not fluctuate as a result of the value of the emission current.

When the emission current is large, as indicated in Fig. 14, it is possible to use a driving method with a self-bias resistor R_{SB} in series to the cathode in order to obtain an emission current with little noise. Fig. 15 shows such anode characteristics. A 2 MΩ self-bias resistor R_{SB} was inserted in series with the cathode for stabilization of the emission current I_E. When V_{KG} = - 270 V, the emission current is 10 μa. Based on this graph, the values obtained where Gm = 10 nS and μ = 1.5.

The characteristics have been summarized in Table 1. Among the tetrode devices, A corresponds to Fig. 12 and B corresponds to Fig. 15.

Table 1

Device		Gm	μ	Transfer characteristics
Desired characteristics		> 1 mS	> 100	Linear
Tetrode device	A	0.2 nS	1	Nearly linear
		V_{AG} = 300 V, V_{CK} = 150 V,		I_E = 1 μA
	B	10.0 nS	1.5	Nearly linear
		V_{AG} = 300 V, V_{CK} = -50 V,		I_E = 10 μA
Triode device		2.0 nS	> 100	Non-linear
		V_{AG} = 300 V, V_{CK} = 120 V,		I_E = 1 μA

Fig. 16 is a circuit diagram with a pentode field electron emission device wherein a screen electrode S has been added to the tetrode field electron emission device described above. In Fig. 16, A is the anode, S is the screen electrode, C is the control electrode, G is the gate electrode and K is the cathode. Fig. 17 shows the anode characteristics of this pentode. They were measured under the following conditions: number of cathode projections 10,000, V_{KG} = 140 V, cathode current I_K = 20 mA, screen electrode voltage V_{SG} = 100 V and load resistor R_L = 1 kΩ. In Fig. 17, if a load of R_L = 80 kΩ is applied (shown by the broken line), the amplification rate is four fold. The operating point at this time is at V_i = - 40 V. A pentode is characterized by that the anode current does not fluctuate because even if the anode current changed, the electric field near the control electrode would not change due to the existence of the screen electrode. That is, the anode resistance Ra will increase as indicate below:

$$Ra = \Delta V_A / \Delta I_A$$

As the next embodiment of the present invention a hexode field electron emission device and a manufacturing process therefor will be described. Figs. 18(A), (B) and (C) are a plan view, a cross-section along line B-B in Fig. 18(A) and cross-section along line C-C in Fig. 18(A), respectively. This hexode field electron emission device comprises control electrode 6, anode 7 and, inbetween these, screen electrode 50 and suppressor electrode 53. In addition, control electrode 6 and screen electrode 50 are equipped with column-shaped control electrode portions 64 and column-shaped screen electrode portions 65, which are formed on top of control electrode 6 and screen electrode 50, respectively. These electrode portions are formed so that they extend beyond the plane or level of cathode 3, i.e. their height is at least higher than the film thickness of island-shaped insulating layer 2.

Control electrode portions 64 have a frustro-conical shape with a middle diameter of 3 μm and a height of 5 μm. They are provided at a 10 μm pitch and are located about 10 μm away from emission projections 4, registered to about the middle between two emission projections. Screen electrode portions 65 have a tapered plate shape with a width of 5 μm, a middle thickness of 3 μm and a height of 5 μm. Like control electrode portions 64, the screen electrode portions 65 are provided at a pitch of 10 μm. Suppressor electrode 53 has a width of 5 μm and is located between anode 7 and screen electrode 50. Its distance from screen electrode 50 is about 20 μm and its distance from anode 7 about 50 μm.

Cathode 3 has eight emission projections 4 formed at a 5 μm pitch. The thickness of island-shaped insulating layer 2 is 500 nm. Gate electrode 5 is formed to be self-aligned with cathode 3. The distance from emission projections 4 is 300 nm. The width of gate electrode 5 in the region of emission projections 4 is about 2 μm. The distance from the control electrode is 4 μm.

The electrons emitted from cathode 3 du to the electric field of gate el ctrod 5 are controlled by the electric field of control electrode 6, and this limits the amount of electrons that reach anode 7. Screen l ctrod 50 is maintained at a constant bias to pr vent fluctuations of the electric field f control lectrode 6 due to th electric field of anode 7. Suppressor lectrode 53 prevents secondary l ctrons emitted by anode 7 from returning

to the dir ction of control electrod 6.

The process for manufacturing the h xode field lectron emission device of this mbodiment will now b described with r ferenc to Figs. 19(A) through (G) which are cross-sectional vi ws of th device after respective major process steps.

First, an insulating layer 8 and a cathode layer 9 are formed in sequence on the surface of flat substrate base 1. Then photoresist layer 11 is formed (Fig. 19(A)). Flat substrate base 1 is made of alumina. Because a ceramic substrate base such as an alumina substrate is highly insulating and has a large thermal conductance ratio, it is excellent as a substrate base for a high power field electron emission device. Instead of this substrate base, a semi-insulating GaAs substrate base or a diamond substrate may also be used. Insulating layer 8 is made of a 500 nm thick silicon dioxide thin film. Cathode layer 9 is made of a 100 nm thick tantalum (Ta) thin film. Photoresist layer 11 is used to form cathode 3.

Next, cathode layer 9 is processed by means of excess-etching to form first cathode layer 3a (Fig. 19(B)). Dry etching was used as etching method for excess-etching. After excess-etching in CF_4/O_2 (120/100) gas and RF power of 700 W for 25 minutes, cathode layer 9 will be excess-etched to 1 μm to form emission projections 4 with a tip curvature radius of 30 nm.

Next, the insulating layer 8 is etched in part to form island-shaped insulating layer 2 and to remove photoresist layer 11 (Fig. 19(C)). The method of forming insulating layer 2 is the same as that described in the previous embodiment.

Next, a column formation layer 56 is formed (Fig. 19(D)). Column formation layer 56 is made from a photosensitive polyimide resin of 5 μm thickness and formed by means of a coating method. As photosensitive polyimide resin, for example, negative type PI-410 (manufactured by Ube Kosan) can be used. Instead of this type of organic material, inorganic materials can also be used as a material for column formation layer 56.

Next, column formation layer 56 is photo-etched to form control electrode portion carriers 64′ and screen electrode portion carriers 65′ (Fig. 19(E)). If column formation layer 56 is not made of a photosensitive material but of some other organic material or inorganic material, an anisotropic etching method such as RIE (Reactive Ion Etching) is suitable instead of photo-etching.

Next, a gate electrode layer 133 is formed using directional particulate deposition. (Fig. 19(F)). Sputtering is used in this case as the particulate deposition method to form thin film gate electrode layer 133 made of tantalum (Ta) with a film thickness of 200 nm. During this step control electrode portion carriers 64′ and screen electrode portion carriers 65′are covered on top and on the sides by gate electrode layer 133.

Finally, gate electrode layer 133 is etched to form second cathode layer 3b, gate electrode 5, control electrode 6, column shaped control electrode portions 64, screen electrode 50, column shaped screen electrode portions 65, suppressor electrode 53 and anode 7 (Fig. 19(G)). If control electrode portion carriers 64′ and screen electrode portion carriers 65′ are made of an organic material, they may be removed after forming column shaped control electrode portions 64 and column shaped screen electrode portions 65 to allow maintaining a high vacuum condition. One method for removing these carriers is as follows: First, the surface of flat substrate base 1 is coated with a resist. At this time, the thickness of the resist on top of column shaped control electrode portions 64 and column shaped screen electrode portions 65 becomes thinner than in other areas. Next, when the resist is etched by means of dry etching the gate electrode layer 133 on top of the said electrode portions 64 and 65 will be exposed. When the gate electrode layer 133 is then etched away in these portions, the top portions of the column shaped control electrode portions 64 and the column shaped screen electrode portions 65 will be removed exposing the carriers 64′and 65′. These carriers are then removed using a solvent. Because the column shaped electrode portions 64 and 65 manufactured in this manner are hollow and do not have organic materials within them that may become sources of outgassing a high vacuum condition can be created and maintained by means of heating exhaustion.

Fig. 20 is a schematic angular view of a hexode vacuum tube that uses the hexode field electron emission device of this embodiment. In this case, the hexode field electron emission device is vacuum packed into a metal cap. That is, the flat substrate 111 having the hexode field electron emission device on it is fixed in place by a hermetic seal. Each electrode and the hermetic pins 161 are connected through respective wires 162. Hermetic seal 160 and cap 163 are sealed in a vacuum to form a vacuum space 164 within cap 163. In order to maintain a high vacuum, a getter material 165 is provided on the inner wall of cap 163 and activated as mentioned before.

Fig. 21 shows a circuit diagram of a cathode grounded type voltage amplifier using a hexode vacuum tube with a hexode field electron emission device as described above. The hexode vacuum tube shown in Fig. 21 is indicated by a symbol mark 66 shown in the middl of Fig. 22. It includ s cath de 3, gate lectrod 5, control electrode 6, screen el ctrode 50, suppr ssor lectrode 53 and anode 7 sealed insid a vacuum space 164. Cathode 3 and suppressor electrode 53 are grounded. A voltage source 26 is connected to gate lectrod 5 to apply a positive bias gate voltag V_{GK} to gate electrode 5. A voltag source 25 and an input signal voltage

source 24 ar connected in series to control electrode 6 to apply to control el ctrode 6 an input signal voltage V_i superposed to a control bias voltag V_{CK}. A voltage source 27 is connected via a load resistor 28 to anode 7 to apply anod voltage V_{AK}. A desired positive bias can b applied to screen lectrod 50. Howev r, for th sake of simplicity in terms of th number of power supply sources and th number f lines, screen el ctrod 50 is connected to gate 5 to have the same bias as gate electrode 5, namely V_{GK}. Cathode 3 and suppressor electrode 53 and gate electrode 5 and screen electrode 50 might be connected to each other, respectively, on the surface of flat substrate base 1 or inside the vacuum tube. Although this embodiment is a hexode, as a result of the above electrical connections, the number of pins and the number of power supplies are the same as with the tetrode vacuum tube already described above.

Next, the method of driving the hexode field electron emission device will be described. First, if a constant gate voltage V_{GK} is applied to gate electrode 5, a constant amount of electrons will be emitted from cathode 3. As long as gate voltage V_{GK} does not change, the amount of emitted electrons will remain constant. In this condition, with anode voltage V_{AK} being held constant, if input signal voltage V_i with DC bias V_{CK} added to it, is applied to control electrode 6, the anode current will be controlled in proportion to the input signal voltage and amplified input signal voltage will be obtained as output signal voltage V_o at terminal 29 using load resistor 28. The field effect of control electrode 6 on the electrons will be the same as that described in the previous embodiment. Screen electrode 50 will prevent field fluctuations due to voltage fluctuations in the vicinity of control electrode 6. It also has the function of improving the anode resistance and the frequency characteristics. Suppressor electrode 53 prevents secondary electrons generated by anode 7 from flowing in the direction of control electrode 6.

When the hexode field electron emission device was driven at V_{AK} = 300 V, V_{GK} = 160 V, V_{CG} = 60 V and R_L = 1 GΩ (R_L is the value of load resistor 28), a voltage amplification rate of μ = 8 was obtained. In this case, the mutual conductance was Gm = 2 x 10^{-9}S. The frequency characteristics improved twofold compared to the tetrode field electron emission device described in the embodiment above. This is believed to be due to the anode screening effect of screen electrode 50.

Fig. 22 shows another circuit diagram of the hexode field electron emission device. In Fig. 22, A is the anode, SP the suppressor electrode, S the screen electrode, C the control electrode, G the gate electrode and K the cathode. Fig. 23 shows its output characteristics (anode characteristics). The characteristics of Fig. 23 were measured under the following conditions: 10,000 cathode emission projections, V_{KG} = -140 V, cathode current I_K = 20 mA, V_{SG} = 100 V and R_L = 1kΩ. As will be clear from comparing Fig. 23 to Fig. 17, the anode resistance is further increased as a result of the existence of the suppressor electrode and the saturation region is shifted to lower anode voltages V_{AG}. The anode resistance is 8 MΩ.

This invention does not only apply to the flat devices described above. It can also be applied to vertical devices. As one example, a vertical tetrode field electron emission device formed on a silicon single crystal substrate will be described in the following embodiment.

Fig. 24 in a schematic view of the general construction of the vertical tetrode field electron emission device of this invention. The device chiefly comprises a conductive flat substrate base 40 which is made of an n-type single crystal silicon substrate with a (100) surface, a cathode 41 formed on the surface of flat substrate base 40, a first insulating layer 42, a gate electrode 43, a second insulating layer 44, a control electrode 45 and an opposing substrate 46 having an anode 47 formed on its surface facing substrate base 40. Space 48 between the substrates is evacuated.

Cathode 41 is formed on the surface of flat substrate base 40 and projects upward in a vertical direction in the drawing. Cathode 41 has a tapered or cone shape as shown in the drawing. The first insulating layer 42 is formed on the surface of flat substrate base 40 and has an opening around the circumference of cathode 41. The gate electrode 43 is formed on the surface of the first insulating layer 42 and also has an opening around the circumference of cathode 41. The second insulating layer 44 is formed on the surface of gate electrode 43 and has an opening around the circumference of cathode 41. The control electrode 45 is formed on the surface of the second insulating layer 44 and has an opening around the circumference of cathode 41.

Since cathode 41 is fabricated by means of anisotropic etching of flat substrate base 1, it has a generally conical shape, the cone axis being perpendicular to the surface of flat substrate base 40. Cathode 41 has a height of about 1.2μm. Its cross sectional apex angle is about 90°. In this invention, a cathode formed by a method other than anisotropic etching of flat substrate base 40 may also be used, i.e., the cathode may also be a Spindt type (see Journal of Applied Physics, Vol. 47, No. 12, December 1976, pages 5248 to 5283). The first and second insulating layers 42 and 44 are made of silicon dioxide thin films of a thickness of 600 nm and 3 μm, respectively. Th diameter of th openings is approximately the same for both insulating lay rs, nam ly around 3 μm. Gat lectrode 43 and control electrod 45 are made from molybdenum. Their film thickn sses are 200 nm and 300 nm, respectively. The diameter of the opening In each l ctrode is about the same, nam ly about 1.2 μm. Flat substrate base 40 and opposing substrat 46 are h ld togeth r by means of a support formed

around their periphery (not shown in the Figure). The thickness of the vacuum space 48 (distance between control electrode 45 and anode 47) is 50 μm. For anode 47, an aluminum thin film or a transparent conductive film is used.

As to the operating functions of this tetrod fi ld lectron mission d vice, when a positive bias is appli d to gate electrode 43, electrons are field emitted from the projecting tip of cathode 41. These emitted electrons pass through the openings of gate electrode 43 and control electrode 45 and arrive at anode 47. However, the amount of electrons that are able to reach anode 7 (anode current) can be controlled by the voltage of control electrode 45. The anode current control by means of the field effect of control electrode 45 is the same as the control mechanism described in the first embodiment. Therefore, there is a linear region in which the voltage of control electrode 45 and the anode current are in a proportional relationshlp. That is, when the voltage of control electrode 45 is a high negative voltage, a negative bias gradient is created from control electrode 45 in the direction of cathode 41 and the emitted electrons are bounced back in the direction of gate electrode 43. In such a case, the anode current is small. However, when the voltage of control electrode 45 is a high positive voltage, a positive bias gradient is created. Many electrons can pass through this and a large anode current is obtained.

The basic structure of the present embodiment of the invention has been explained above with reference to one cathode 41, extending into a hole formed by insulating layers 42 and 44 and electrodes 43 and 45. It should be noted that substrate base 40 of this embodiment may be provided with one or more cathodes 41 each extending into a respective hole in elements 42 to 45.

The electrical characteristics of the tetrode field electrode emission device of this embodiment in which 10,000 cathodes 41 were formed were measured. In a cathode grounded circuit, when the gate voltage was 120 V an emission current of 3 mA was obtained. The change in the anode current relative to a change in the voltage of the control electrode, that is the mutual conductance was Gm = 20 μS. The ineffective current that flowed to gate electrode 43 was 1 % or less of the anode current, thus, excellent characteristics where obtained.

Further, it is clear, that if a screen electrode and suppressor electrode are added to the tetrode field electron emission device of this embodiment, its electrical characteristics can be further improved. In this embodiment anode 47 is formed on the opposing substrate base 46. However, it may also be formed on the surface of flat substrate base 40. In this case, control electrode 45 can be placed between anode 47 and gate electrode 43. For example, it may be placed in the middle of vacuum space 48. In addition, in order to reduce the capacitance between the anode and the cathode (and/or the gate electrode) and to improve the frequency characteristics and the breakdown voltage, it is appropriate to make the cathode to be comprised of a thin film layer on an insulating substrate and to form the anode of the same layer so as to surround the cathode in order to remove overlapping regions between the anode and the cathode (and/or the gate electrode). In such a case an insulating flat substrate base 40 would be used.

As with the tetrode field electron emission device of this embodiment the multiple electrode field electron emission device is either formed so that gate electrode 43 is perpendicular to the direction of electron emission from cathode 41 and formed so that the opening of gate electrode 43 surrounds the route of flow of the electrons, reducing the ineffective current that flows to gate electrode 43 and yielding excellent power efficiency. The reason for this is that the emitted electrons need to travel a short distance only corresponding to the thickness of gate electrode 43 to traverse the gate electrode through its opening. This is also because the emitted electrons have only a small probability of impacting with gate electrode 43 because they pass through the center region of the opening. It would be very effective to apply this type of structure to a horizontal multiple electrode field electron emission device.

In order to increase the mutual conductance of a horizontal multiple electrode tube, for example, it is necessary to devise a gate electrode structure in the tetrode field electron emission device shown in Fig. 1 so that the emission surface area of cathode 3 is larger. However, if the emission surface area is increased, there will be an increase in the number of electrons that flow to gate electrode 5. As a result, the problem is, that it is difficult to obtain power amplification that has high performance.

Fig. 25 is an angular fractional view of an enlarged multiple electrode electron emission device having a gate electrode 51 with ring-shaped electrode portions 52 each providing an opening 52a. The openings are registered with the emission projections 4 of cathode 3. Cathode 3 has the same structure as that shown in Fig. 1. By this structure of the gate electrode, the gate current and the control current are reduced by passing the electrons that are emitted from emission projections 4 through the openings 52a of the ring-shaped gate electrode portions 52, allowing a reduction in parasitic current and an increas in input resistance.

The gate lectrode portions 52 are not limited to the shap shown in Fig. 25. Th structur should be such that such lectrode portion provides an opening through which electrons emitted from a respectiv emission projection 4 can pass, the opening being surrounded by conductive material being at the sam electrical bias all around the opening. The opening may be circular, elliptic, square-like or rectangular-lik in cross-section.

Such electrode portion need not necessarily be provided for each of the emission projections. It is possible, for example, that only for every second emission projection 4 a corresponding electrode portion with such an opening is provided.

The poor power conversion ratio resulting in case of $I_G > I_A$, as shown in Fig. 8, can be improved by providing a gate electrode 51 with such electrode portions having an opening, and a field electron emission device having linear input and output electrostatic properties can be obtained due to the existence of a control electrode. In Fig. 25, 61 is the control electrode and 7 is the anode. As shown in Fig. 25, control electrode 61 may be structured to have electrode portions 62 with openings 62a similar to the electrode portions 52 of gate electrode 51, to allow emission current to pass through. However, this is not a necessary requirement and the control electrode may also be a flat electrode like that shown in Fig. 1.

A tetrode field electron emission device having a gate electrode structure like that shown in Fig. 25 has the linear input and output relationship of the device shown in Fig. 1 and furthermore is characterized by a drastically reduced gate current (1/10 or less of the anode current) and a drastically reduced gate ineffective current.

The device shown in the angular view of Fig. 26 differs from that of Fig. 25 in that control electrode 61 has column-shaped control electrode portions 63. These control electrode portions 63 are positioned midway between imaginary straight extension lines extending from the emission projections 4 toward the anode 7.

In the multiple electrode field electron emission device of this invention, the number of electrodes is optional. Quite naturally it could be a hexode field electron emission device, for example. It is possible to have the structure of gate electrode 5 of the hexode field electron emission device shown in Figs. 18(A) through (C) replaced by that of gate electrode 51 shown in Fig. 25. In such a case, the electrons that are emitted from emission projections 4 will be controlled by the electric field of control electrode 6, and the amount of electrons that reach anode 7 would also be controlled. Screen electrode 50 will be maintained at a constant electric bias preventing fluctuation in the electrical field of control electrode 6, which would otherwise be caused by the electric field of anode 7. Suppressor electrode 53 will prevent secondary electrons generated by anode 7 from returning in the direction of control electrode 6.

However, the three-dimensional gate electrode structure described above has problems in terms of manufacturing. For example, the gap control is difficult for thin film manufacturing technology. Further, the distribution of the electric field between the cathode and the gate electrode is not uniform, and there is a limit to the I_A/I_G characteristics. Moreover, the manufacturing process requires four photo mask steps, necessitating complex manufacturing technology. For these reasons and based on the objective of providing a three-dimensional electric field distribution between the cathode and the gate electrode, it is desirable to use a gate electrode with a uniform structure, and that structure should be such that it allows self-alignment (even if the position of one of the electrodes has an offset, the other electrode will be formed in a position corresponding to that offset position).

In the following, a multiple electrode field electron emission device that resolves these technical problems and the manufacturing process of that device will be explained. It forms an extremely stable electrode and greatly improves the I_A/I_G characteristics. This is because it is a multiple electrode field electron emission device that comprises a cathode formed on top of an insulating layer which in turn is formed on the surface of an insulating flat substrate base, and having a plurality of emission projections that overhang from said insulating layer, comprises anodes that are formed on the surface of said flat substrate base and which collect the emitted electrons, and comprises a number of column-shaped gate electrodes that are formed inbetween the cathodes and the anodes. The emission projections are located between adjacent gate electrodes and the shape of the gate electrodes corresponds to that of the emission projections on the cathode.

Fig. 27(a) is a schematic plan view of this new multiple electrode field electron emission device. Fig. 27(b) is a cross-sectional view along line a-a in Fig. 27(a). Fig. 27(c) is a cross-sectional view along line b-b of Fig. 27(a). Fig. 27(d) is an angular view of a section of the device shown in Fig. 27(a).

In this device, cathode 303, gate electrodes 305 and anode 7 are on the surface of a flat substrate base 1 which is made of quartz. Cathode 303 is formed of a thin film (having a thickness of for example 200 nm) on the surface of a silicon dioxide island-shaped insulating layer 302. The side of cathode 303 facing anode 307 has a saw-tooth like shape with emission projections 4 overhanging insulating layer 302 as shown in Fig. 27(b). Cathode 303 may be a one or a multi layer structure of thin films (for example, it may comprise a molybdenum thin film on top of a tungsten thin film). Emission projections 4 project in the direction of gate electrodes 305 in parallel to the surface of flat substrate base 1. Insulating layer 302 does not exist beneath the tip area of emission projections 4. The tip curvature radius of the emission projections 4 within the plane of the cathode is 40 nm or less.

Gate electrodes 305 are formed such that they self-align to cathode 303. As shown in the drawing, the gate electrodes 305 have a shape of a pentagonal column, and the angle Θ of the corner facing cathode 303 is for example 60 to 90°. The emission projections are formed to extend in the space between adjacent gate elec-

trodes 305. Therefore, the electric field distribution in the vicinity of the emission projections 4 is laterally symmetrical. If the height G of the pentagonal column of each gate electrode 305 is larger than that of cathode 303, the distribution of the electric field in the area of emission projections 4 will not only be laterally symmetrical but also approximately uniform in the vertical direction. As a result, the electrons emitted from emission projections 4 due to the electric field between cathode 303 and gate electrode 305 will pass through the space between adjacent gate electrodes 305 and arrive in an efficient manner at anode 307. This will allow a remarkable reduction of the parasitic current flowing into the gate electrode. That is, the I_A/I_G characteristics (power conversion ratio) is remarkably improved.

The structure of gate electrodes 305 is not limited to a pentagonal column. It should be a column shape with which a symmetrical electric field is formed in the vicinity of the emission projections 4 and which allows the emitted electrons to efficiently travel to anode 307 (for example, it could be a triangular column or a column with a curved back).

The foregoing embodiment is a flat triode field electron emission device. However, according to the invention, this embodiment can be modified to a tetrode or pentode type field electron emission device.

Reference numeral 71 in Fig. 27 denotes a gate electrode interconnection. To give an example of the dimensions in each section, distance A between the gate electrodes 305 is 3 μm. Length B of the pentagonal column of gate electrode 305 is 5 μm. Width C is 7 μm. The gap D between gate electrode 305 and cathode 303 is 1.5 μm. The thickness E of the island-shaped insulating layer 302 is 0.5 μm. The thickness F of cathode 303 is 0.1 μm.

Next, a general description of the manufacturing process of the foregoing embodiment of the invention will be given with reference to Figs. 28, 29 and 30.

First as indicated in the cross-sectional view of Fig. 28(a), a thermal CVD method is used to form a silicon dioxide thin film 311 on the surface of substrate base 1, which is made of quartz, glass, etc. Next, a method such as sputtering is used to form a tungsten layer 312 on top of thin film 311. However, the material for the layer 312 is not limited to tungsten but another material such as tantalum, for example, could be used. After this, as indicated in Fig. 28(b), a resist layer 314 is formed except for resist holes 313 which have the shape of gate electrode columns to be formed. Fig. 28(c) shows the cross-section along line b-b in Fig. 28(b). Then, an etching step using CF_4 gas, etc. is carried out to etch tungsten layer 312 exposed within resist holes 313, as indicated at 315 in Fig. 28(c). Thereby silicon dioxide thin film 311 is exposed as indicated at 316 in Fig. 29(a).

After this, using an HF type etching solution, the exposed silicon dioxide thin film 311 is etched. By excess-etching the reverse taper shape of the silicon dioxide film 311, shown in the cross-sectional view of Fig. 29(b) is obtained. Next, when tungsten layer 312 is etched with a CH_4 type etching solution, the etching of the tungsten progresses to broken lines 317 and 318 shown in Fig. 29(c), and a structure according to Fig. 29(d) corresponding to a sectional view along line c-c in Fig. 29(c) is obtained. This forms the cathode emission projections 319. Since the etch solution distributing from resist holes 313 excess-etches the tungsten layer 312 along the circumference of resist holes 313, the emission projections 319, which are part of the cathode being formed, are etched from the two sides of respective adjacent resist holes 313 so that the tip of each emission projection 319 becomes sharp. Furthermore, the position of the tip has an equal distance to the adjacent resist holes 313. As a result of this manufacturing process, it is possible to have the emission projections 319 formed in such a manner, that they are always positioned in the middle between adjacent resist holes 313, even though there may be an error in the positioning of resist holes 313. Also, the distribution of the electric field formed by emission projections 319 and the gate electrodes is always laterally symmetrical. That is, it is possible to form the cathode and the gate electrodes in a self-aligning manner.

After this, as shown in the cross-sectional view of Fig. 30(a), molybdenum, etc., i.e. the material for forming the gate electrodes is vapor deposited or sputtered to obtain molybdenum films 321 and 322. The shape of molybdenum film 321 and, thus, of a gate electrode in a horizontal cross-section is the same as that of a resist hole 313 (Fig. 29(c)). Depending on the manufacturing conditions of vapor deposition or sputtering, it is possible to form molybdenum film 321 to a height higher than that of tungsten layer 312. After removing molybdenum films 322 and resist layer 314, the result is as shown in Fig. 30(b). Thereby, the cathode and the gate electrodes corresponding to those shown in Fig. 27(c) have been formed. As to the anode in this embodiment, when tungsten layer 312 has been etched away within the region between broken lines 317 and 318 in Fig. 29(c) by excess-etching, the remaining tungsten layer portion beyond broken line 317 and denoted 320 in Fig. 29(c) may be used as the anode, although the anode may also be fabricated separately. The tungsten layer portion 320 may also be used as the control electrode of a multiple electrode field emission device or it may be removed if it is not necessary.

The gate electrode interconnection 71 (Fig. 27(d)) is formed in advance using a photo mask. Therefore, with this manufacturing process, two photo mask steps are necessary only, namely the photo mask step that

patterns the gate electrode interconnection and the photo mask step the forms the resist film 314 shown in Fig. 28(b).

The gate electrode interconnection may be placed wherever desired. When it is located close to the cathode, the electric field betw en the cathode and the gat electrode will increas , r sulting in a d vic having an excellent electric field.

In the process step of Fig. 30(a) of the above described manufacturing process, when the molybdenum film is formed either by vapor deposition or sputtering, sometimes a molybdenum bridge 323 is formed between molybdenum films 321 and 322 as shown in Fig. 31. Since this is not good for the formation of the gate electrodes, the manufacturing process should be one that does not form bridges 323.

An example of such manufacturing process will be explained below. Fig. 32(a) is an enlargement of a part of Fig. 28(c) additionally showing gate electrode interconnection pattern 325 which has been formed in advance on substrate base 1 (aluminum is one of several possible materials for the gate electrode interconnection).

In this condition, when the silicon dioxide layer 311 is excess-etched, as shown in Fig. 32(b), the interconnection pattern is exposed. Therefore, as shown in Fig. 32(c), a thin layer 326 of aluminum is formed on top of the interconnection pattern 325 by means of vapor deposition or sputtering. 327 denotes the aluminum layer formed on top of resist layer 314.

Next, after tungsten layer 312 has been excess-etched (Fig. 32(d)), part of resist layer 314 which is around the periphery of resist hole 328 is removed using oxygen plasma, etc. (Fig. 32(e)). Next, gate electrode metal 329 (which may be aluminum or molybdenum) is formed by means of vapor deposition or sputtering (Fig. 32(f)). After that, resist 314 and layers 327 and 329 on top of it may be removed (Fig. 32(g)). When forming the gate electrodes by means of this manufacturing process, bridges like bridges 323 mentioned above, will hardly be formed because the holes in the resist layer 314 have been widened.

It should be noted that for the sake of simplification the foregoing embodiment has been explained with respect to a three electrode structure, i.e. a triode. It goes without saying that to fabricate a multiple electrode field electron emission device according to the present invention, namely a tetrode, pentode, etc. on the basis of this embodiment, a control electrode, etc. has to be added.

Claims

1. A multiple electrode field electron emission device having a cathode (3) for emitting electrons by means of the field effect, a gate electrode (5) for establishing an electric field between said cathode and said gate electrode, and an anode (7) for collecting the emitted electrons, characterized by additionally having a control electrode (6) placed between said cathode (3) and said anode (7) for controlling the emitted electrons.

2. The device of claim 1 further comprising a screen electrode (50) for electrostatically screening the control electrode (6) and the anode (7) said screen electrode (50) being placed between the control electrode (6) and the anode (7).

3. The device of claim 2 further comprising a suppressor electrode (53) placed between said screen electrode (50) and said anode (7) for controlling secondary electrons emitted from the anode.

4. The device according to claim 1, wherein an island-shaped insulating layer (2a; 2; 202) is formed on the surface of an insulated flat substrate base (1), the cathode (3; 203) is formed on the surface of said insulating layer (2a; 2; 202) and is equipped with emission projection means (4) overhanging said insulating layer, the gate electrode (5; 205) is formed on the surface of said flat substrate base in the vicinity of a region defined by a perpendicular projection of said emission projection means onto the surface of the flat substrate base (1), the anode (7) is formed on a side of the surface of said flat substrate base 1 opposite to that of the cathode (3; 203) with the gate electrode (5; 205) located between the anode and the cathode, and the control electrode (6) is formed on the surface of said flat substrate base 1 between the gate electrode and the anode.

5. The device of claim 4 wherein a screen electrode (50) is formed between the control electrode (6) and the anode (7) on the surface of the flat substrate base (1).

6. The device of claim 5, wherein a suppressor electrode (53) is formed between the screen electrode (50) and the anode (7) on th surface of the flat substrate base (1).

7. The device according to any of claims 4 to 6, wherein the control electrode (6) comprises column-shaped

electrode portions (64) extending from the surfac of the flat substrate base (1).

8. The device according to claims 5 and 7, wherein the screen electrode (50) comprises column-shaped electrode portions (65) xtending from the flat substrate base (1).

9. The device according to any of claims 1 to 3, wherein a vacuum space (48) is formed between a conductive first flat substrate base (40) and an opposing second flat substrate base (46), a cone-shaped cathode (41) is formed on the inner surface of the first substrate base (40) and has a nearly perpendicular cone axis, an insulating layer (42) is formed on the inner surface of said first flat substrate base (40) and has an opening around the circumference of said cathode (41), a gate electrode layer (43) is formed on the surface of said insulating layer (42) and has an opening around the circumference of said cathode (41), an anode layer is formed on the inner surface of said second flat substrate base (46) and a control electrode (45) is arranged between said gate electrode (43) and said anode (47).

10. The device according to any of claims 4 to 8, wherein said emission projection means comprises a plurality of emission projections (4) overhanging from said insulating layer, and said gate electrode (51) has an opening (52a) in at least one location that corresponds to the position of an emission projection (4).

11. The device according to claim 10, wherein said gate electrode (51) has openings (52a) in all of the locations corresponding to said emission projections (4).

12. The device according to claim 10 or 11 in combination with any of claims 4 to 6, wherein the control electrode (61) has one or more openings (62a) respectively corresponding and aligned to said one or more openings (52a) of the gate electrode (51).

13. A process for manufacturing a field electron emission device having cathode emission projection means (4) projecting nearly in parallel to the surface of a flat substrate base (1), said process comprising the steps of

forming an etching mask layer (8) on the surface of said flat substrate base (1),
forming a cathode layer (9) on the surface of said etching mask layer,
depositing and forming an etching passivation layer (10) on the surface of the cathode layer (9),
processing said etching passivation layer to form an etching mask (12) which has projection means corresponding to said emission projection means, and
etching said cathode layer to form the cathode (3a) with its emission projection means (4a) using said etching mask (12).

14. A process for manufacturing a field electron emission device, comprising the steps of

forming an etching mask layer (8) on the surface of a flat substrate base (1),
forming a cathode layer (9) on the surface of the etching mask layer (8),
forming a photoresist pattern (11) on the surface of the cathode layer (9),
processing the cathode layer (9) to assume a shape corresponding to that of the photoresist pattern (11),
processing said etching mask layer (8) using an excess-etching method to form an etching mask (81),
processing the pre-patterned cathode layer (91) to the shape of the etching mask (81) to form a cathode (203a),
removing said etching mask (81) below marginal portions of the cathode (203a) to form said cathode in the shape of an eaves,
forming a gate electrode layer (205, 7) using a particulate deposition method, and
patterning said gate electrode layer to form a gate electrode (205).

15. A multiple electrode field electron emission device having a cathode (3) for emitting electrons by means of the field effect, a gate electrode (5) for establishing an electric field between said cathode and said gate electrode, and an anode (7) for collecting the emitted electrons, characterized in that said cathode (303) is formed on an insulating layer (302) and has a plurality of emission projections (4) overhanging from said insulating layer (302), th insulating lay r being formed on a flat substrat base (1), the anode (307) is formed on th surfac of said flat substrate base (1), and a plurality of column-shap d gate electrodes (305) is formed inbetween said cathode (303) and said anode (307), wherein said emission projections (4) are located in th middle of adjacent gate electrodes (305), ach gate l ctrod (305) proj cting into

the space between adjacent mission projections (4).

16. The device of claim 15, wherein each gate electrode (305) is in th form of a pentagon-shaped column.

17. The device as claimed in claim 15 or 16, wherein the gate electrodes (305) have a height (G) such that they extend beyond the plane of said emission projections (4).

18. A process for manufacturing the multiple electrode field electron emission device of claim 15 comprising the steps of

forming on an insulated flat substrate base (1) an insulating layer (311) and an electrode layer (312) in this sequence,

applying a photoresist (314) on the surface of said electrode layer (312) except for portions (resist holes 313) where the gate electrodes are to be formed,

forming the emission projections by excess-etching the electrode layer (312) and the insulating layer (311) using an etching solution applied via the resist holes (313) that etches beyond the base area of the resist holes, and

forming that column shaped gate electrodes at the locations of said resist holes (313) and removing the resist.

19. The process according to claim 18, wherein prior to forming said gate electrodes said resist holes (313) are widened to have a base area larger than that of the gate electrodes to be formed.

20. A method for driving the multiple electrode field electron emission device of claim 1 or 4, wherein the cathode is grounded, a positive bias gate voltage is applied to the gate electrode, a positive bias anode voltage larger than the gate voltage is applied to the anode and an input signal voltage is applied to the control electrode to control the anode current.

21. A method for driving the multiple electrode field electron emission device of claim 1 or 4, wherein the gate electrode is grounded, a negative bias cathode voltage is applied to the cathode, a positive bias anode voltage is applied to the anode and an input signal voltage is applied to the control electrode to control the anode current.

22. The method of claim 21, wherein said cathode voltage is applied via a resistor to the cathode.

23. A method for driving the multiple electrode field electron emission device of claim 2 or 4, wherein the gate electrode is grounded, a negative bias cathode voltage is applied to the cathode, a positive bias screen voltage is applied to the screen electrode and an input signal voltage is applied to the control electrode to control the anode current.

24. A method for driving the multiple electrode field electron emission device of claim 3 or 4, wherein the cathode and the suppressor electrode are grounded, a gate voltage is applied to the gate electrode and the screen electrode, an anode voltage is applied to the anode and an input signal voltage is applied to the control electrode to control the anode current.

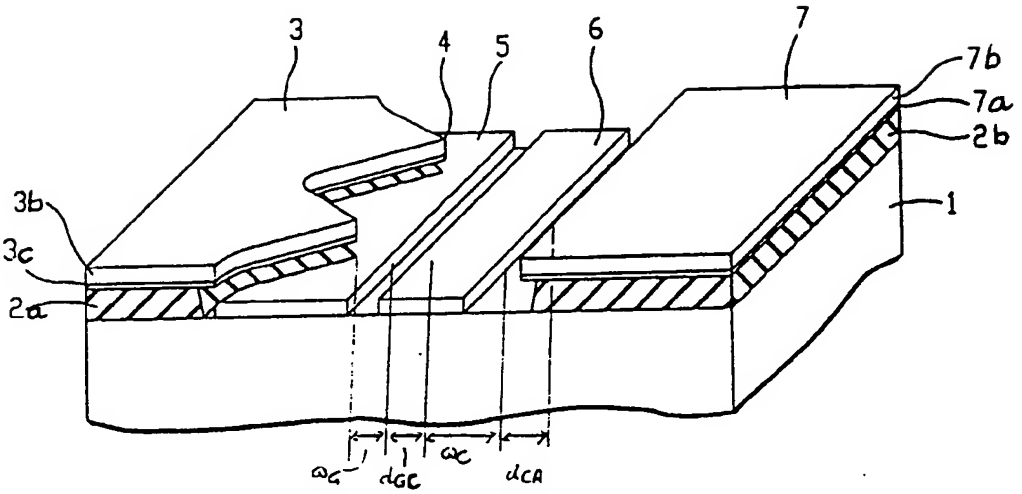


FIG.-1

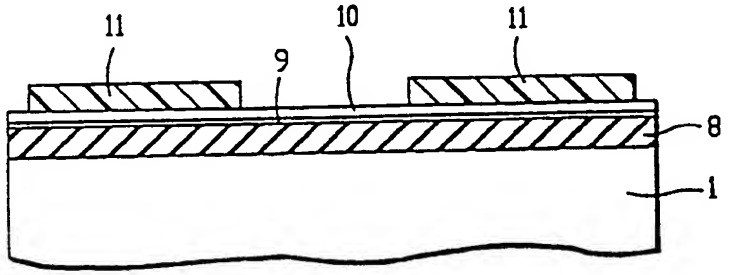


FIG.-2(A)

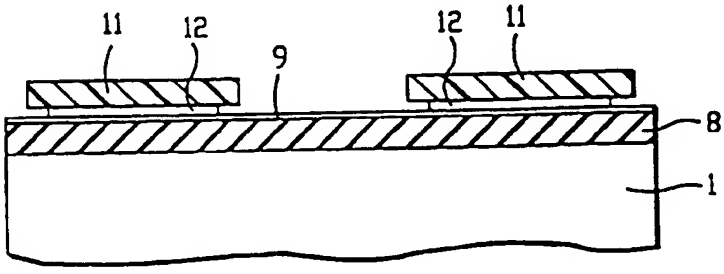


FIG.-2(B)

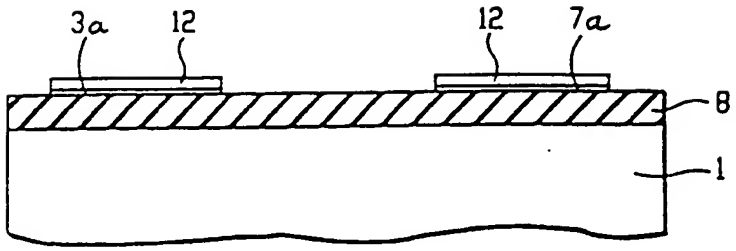


FIG.-2(C)

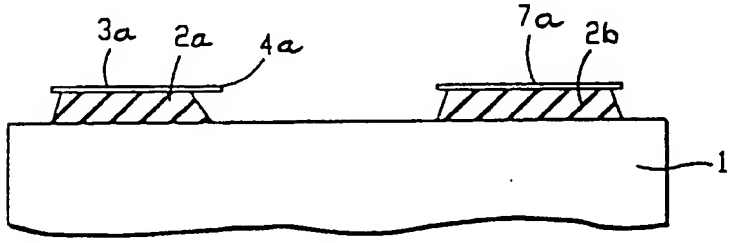


FIG.-2(D)

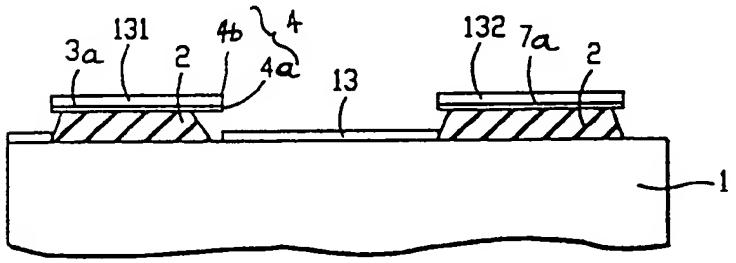


FIG.-2(E)

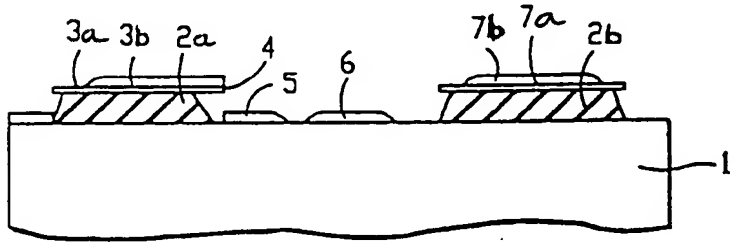


FIG.-2(F)

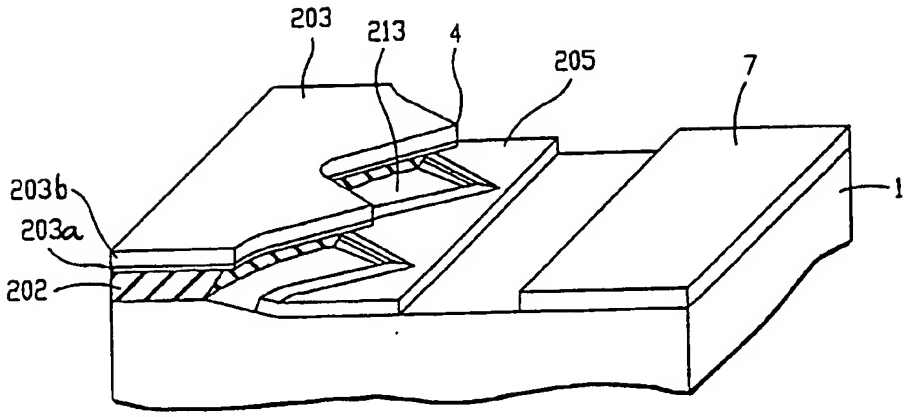


FIG.-3

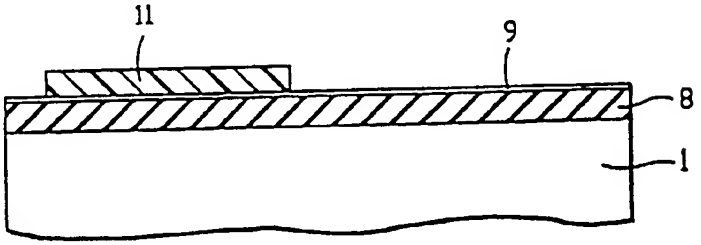


FIG.-4(A)

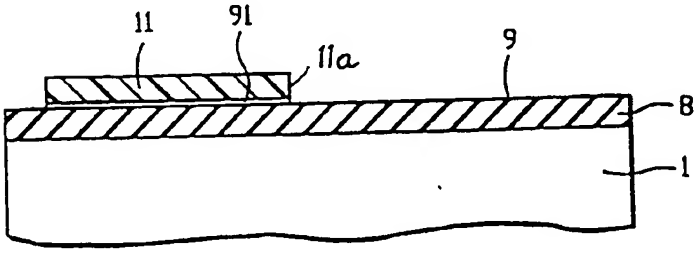


FIG.-4(B)

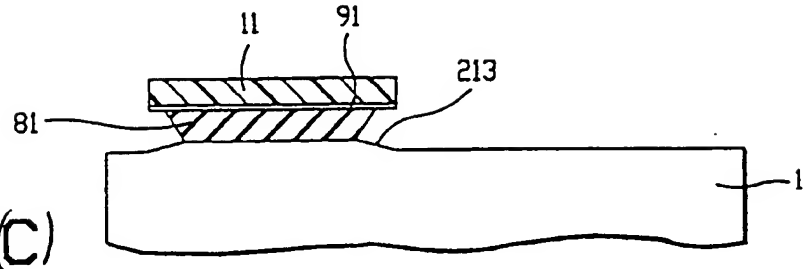


FIG.-4(C)

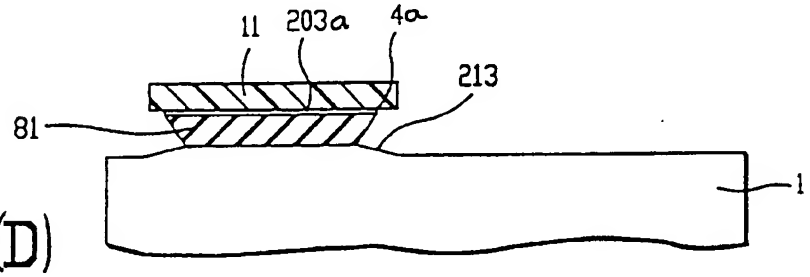


FIG.-4(D)

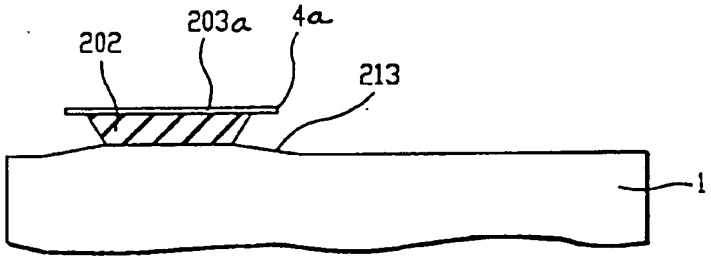


FIG.-4(E)

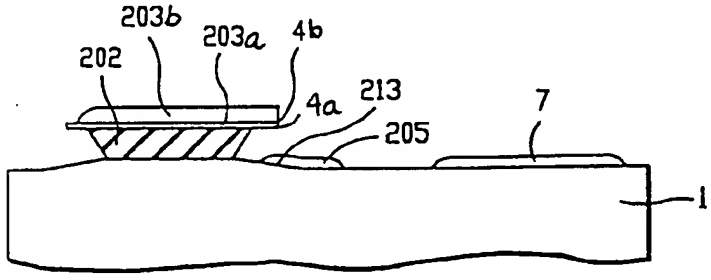


FIG.-4(F)

FIG.-5(A)

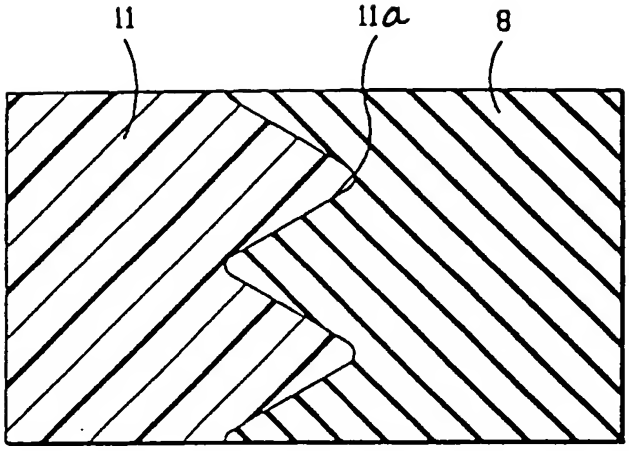


FIG.-5(B)

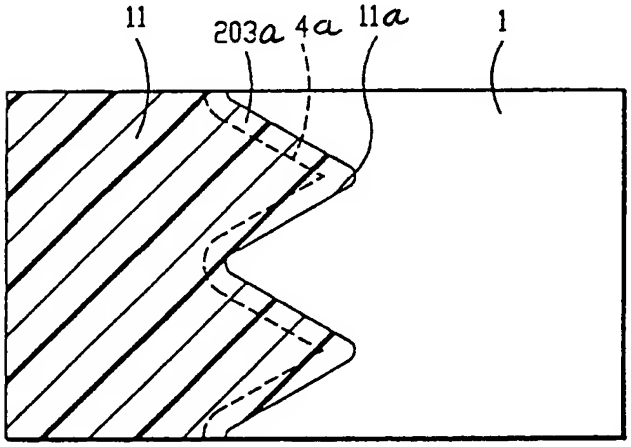
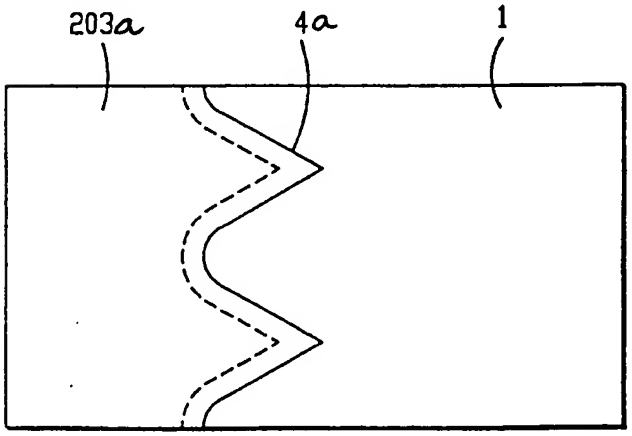


FIG.-5(C)



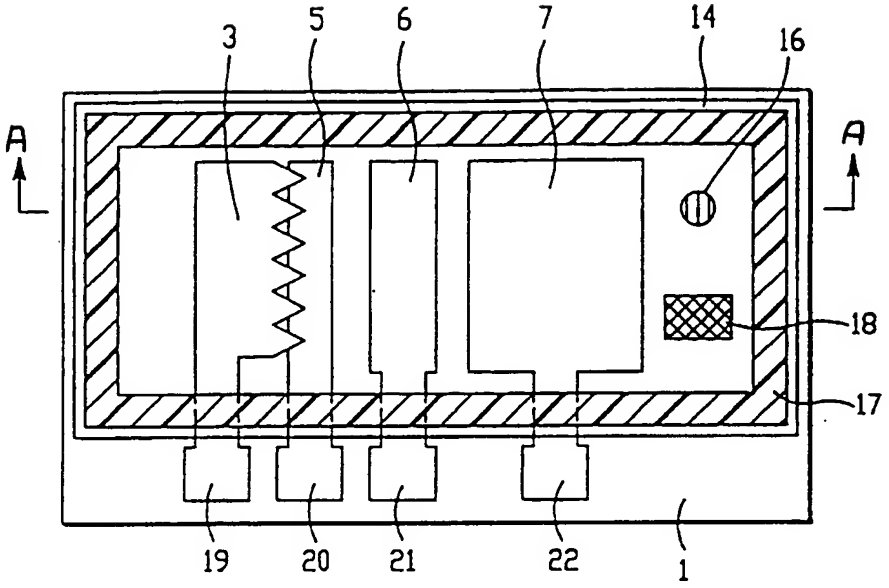


FIG.-6(A)

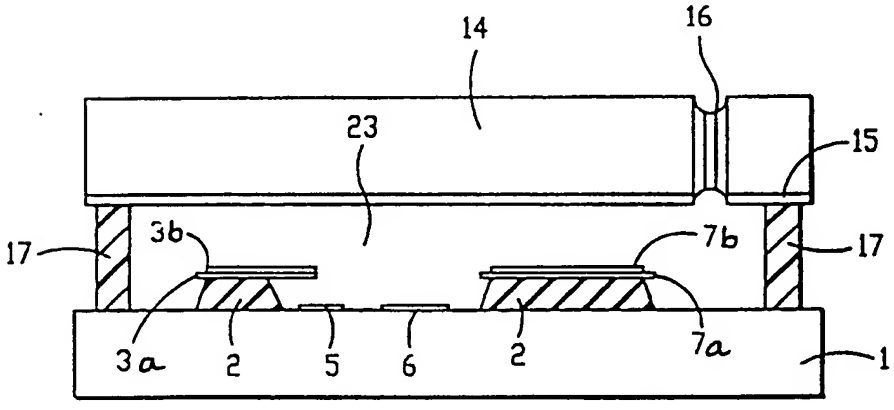


FIG.-6(B)

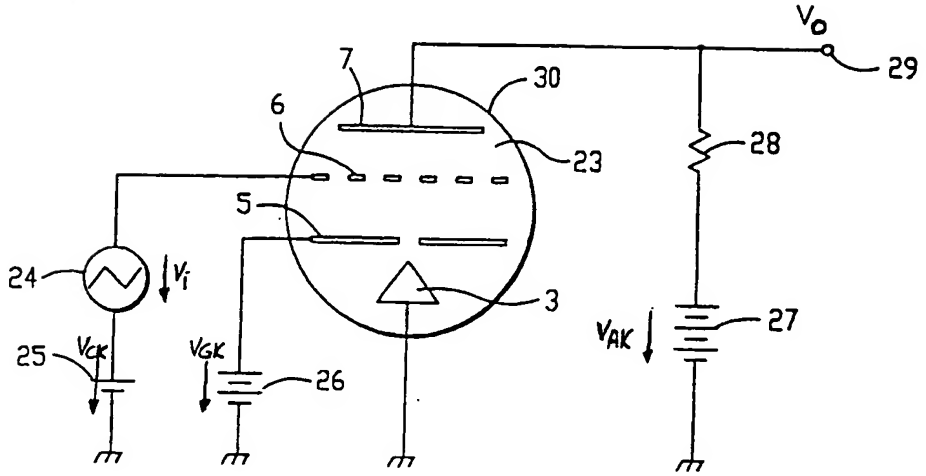
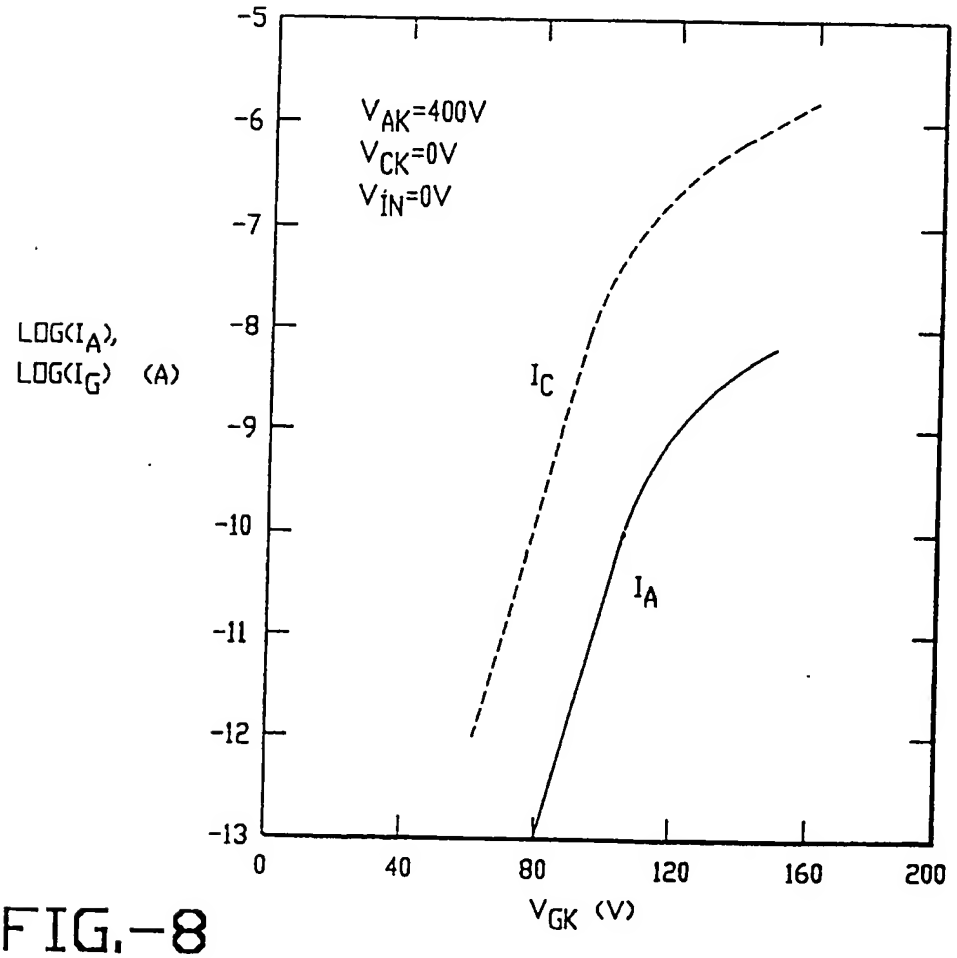

V_o
29
7
30
6
23
28
5
24
V_i
3
V_{AK}
27
25
V_{CK}
V_{GK}
26

FIG.-7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-8
-9
-10
-11
-12
-13
V_{AK}=400V
V_{CK}=0V
V_{IN}=0V
LOG(I_A), LOG(I_G) (A)
I_C
I_A
0
40
80
120
160
200
V_{GK} (V)

FIG.-8

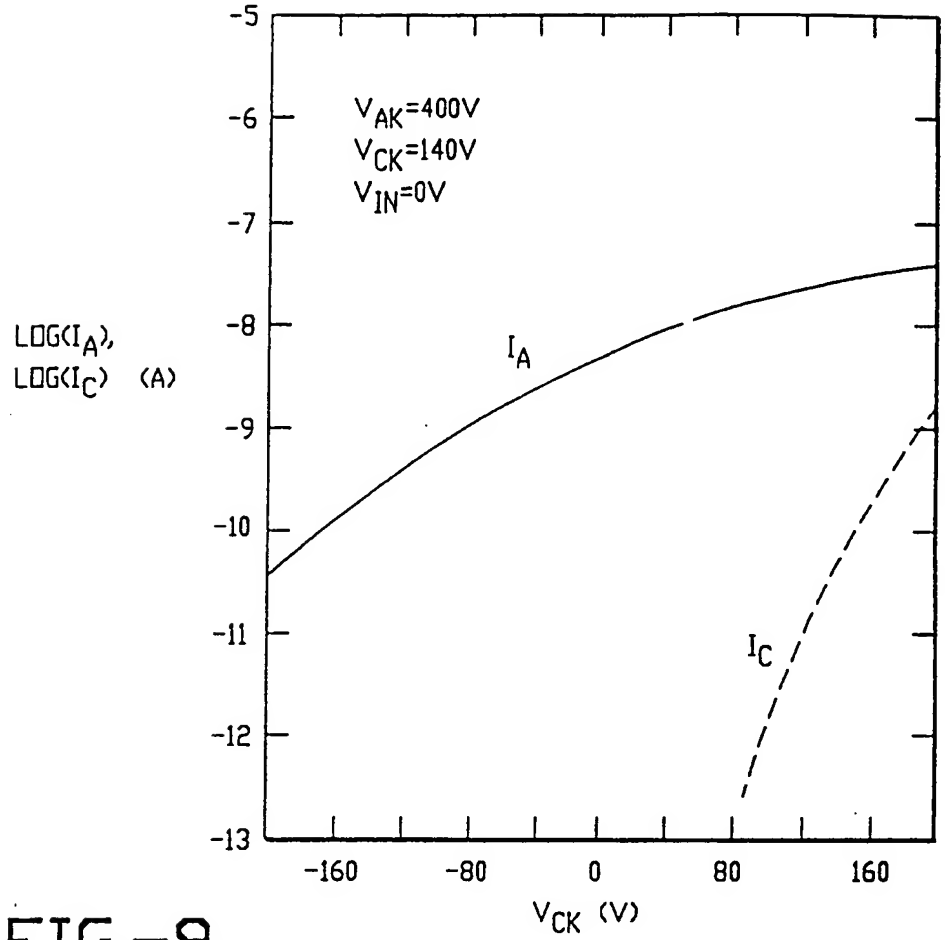

-5
-6
-7
-8
-9
-10
-11
-12
-13
V_{AK}=400V
V_{CK}=140V
V_{IN}=0V
I_A
I_C
LOG(I_A), LOG(I_C) (A)
-160
-80
0
80
160
V_{CK} (V)

FIG.-9

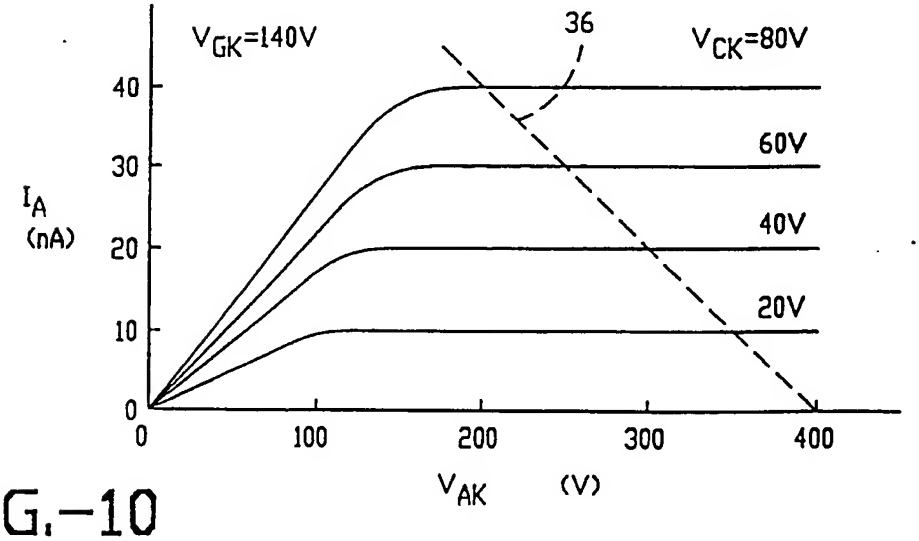

V_{GK}=140V
36
V_{CK}=80V
60V
40V
20V
40
30
20
10
0
I_A (nA)
0
100
200
300
400
V_{AK} (V)

FIG.-10

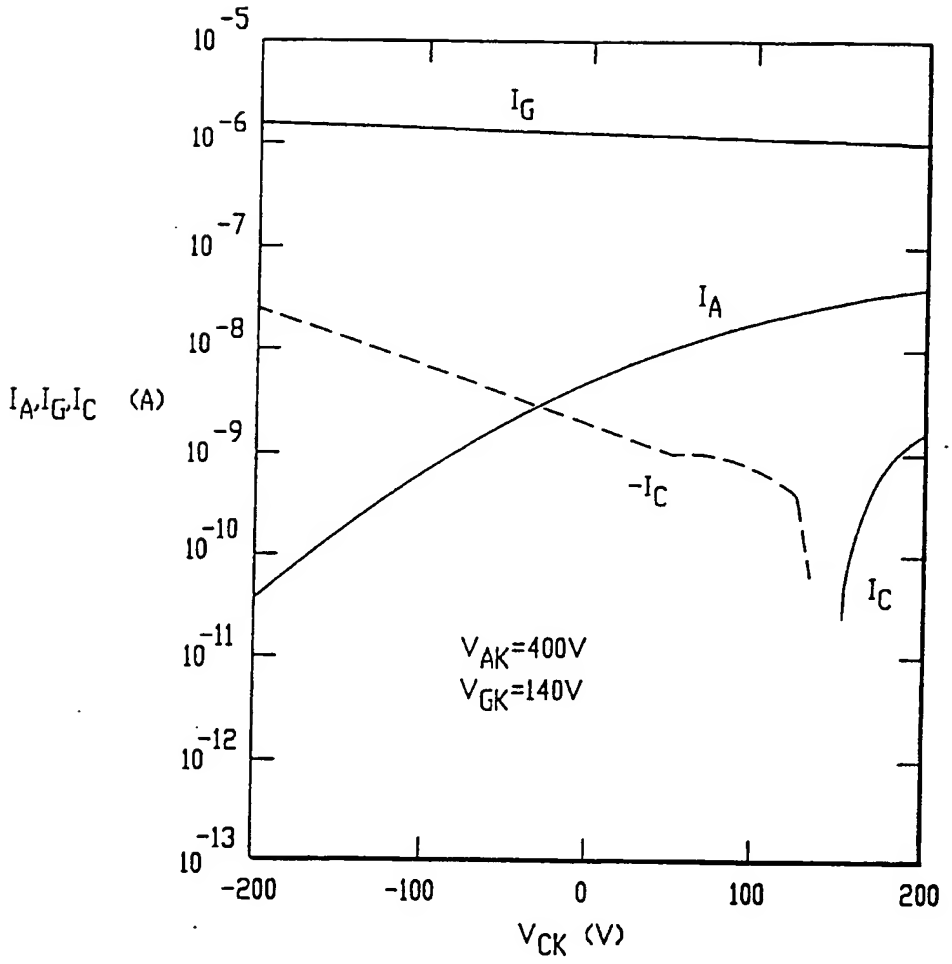

10^{-5}
10^{-6}
10^{-7}
10^{-8}
10^{-9}
10^{-10}
10^{-11}
10^{-12}
10^{-13}
I_A, I_G, I_C (A)
I_G
I_A
$-I_C$
I_C
V_{AK}=400V
V_{GK}=140V
-200
-100
0
100
200
V_{CK} (V)

FIG.-11

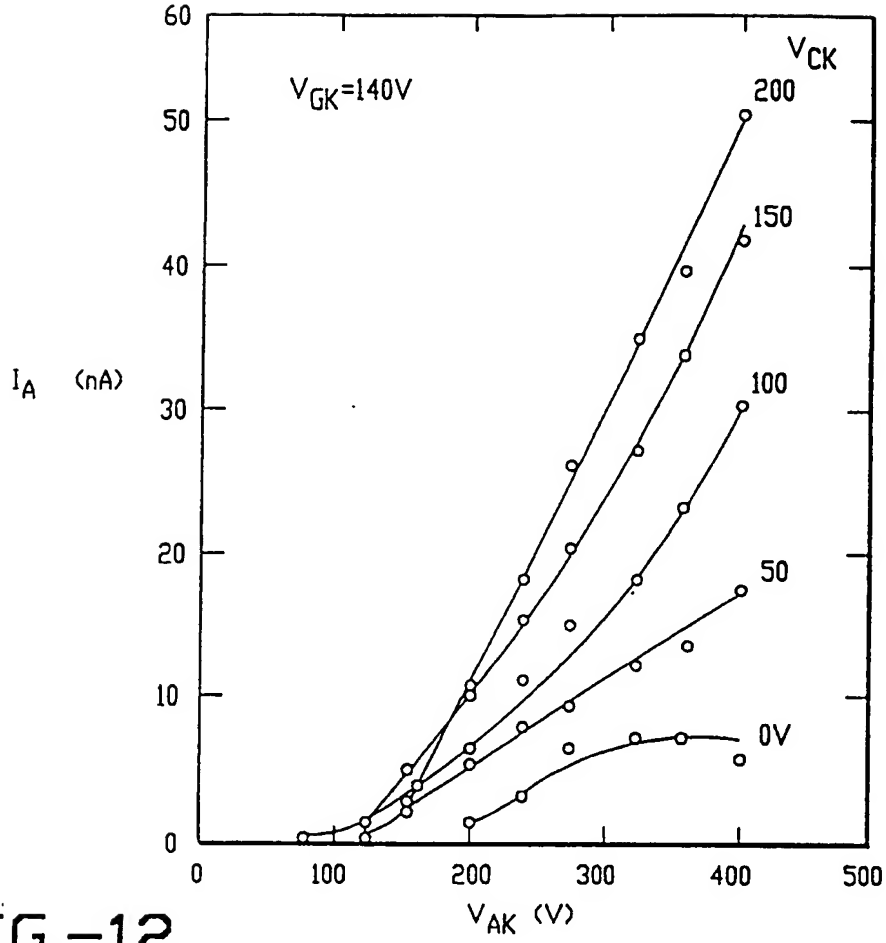

60
50
40
30
20
10
0
I_A (nA)
V_{GK}=140V
V_{CK}
200
150
100
50
0V
0
100
200
300
400
500
V_{AK} (V)

FIG.-12

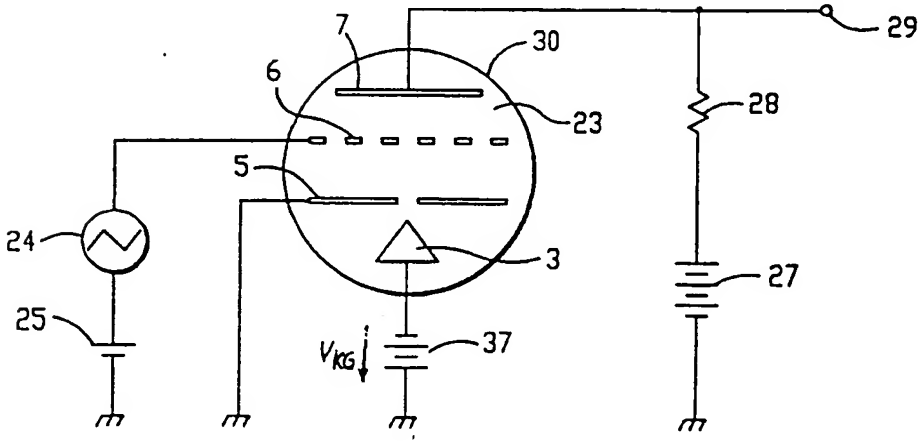

7
30
29
6
23
28
5
24
3
27
25
V_{KG}
37

FIG.-13

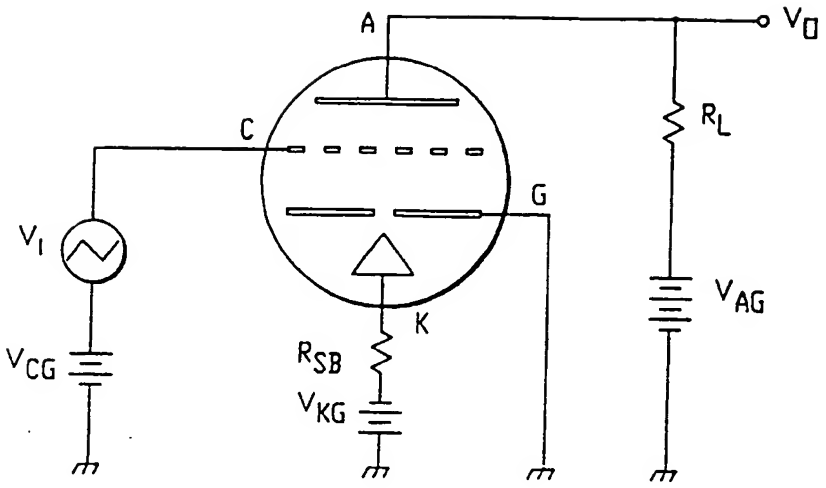

A
V_O
C
R_L
G
V_I
V_{AG}
K
V_{CG}
R_{SB}
V_{KG}

FIG.-14

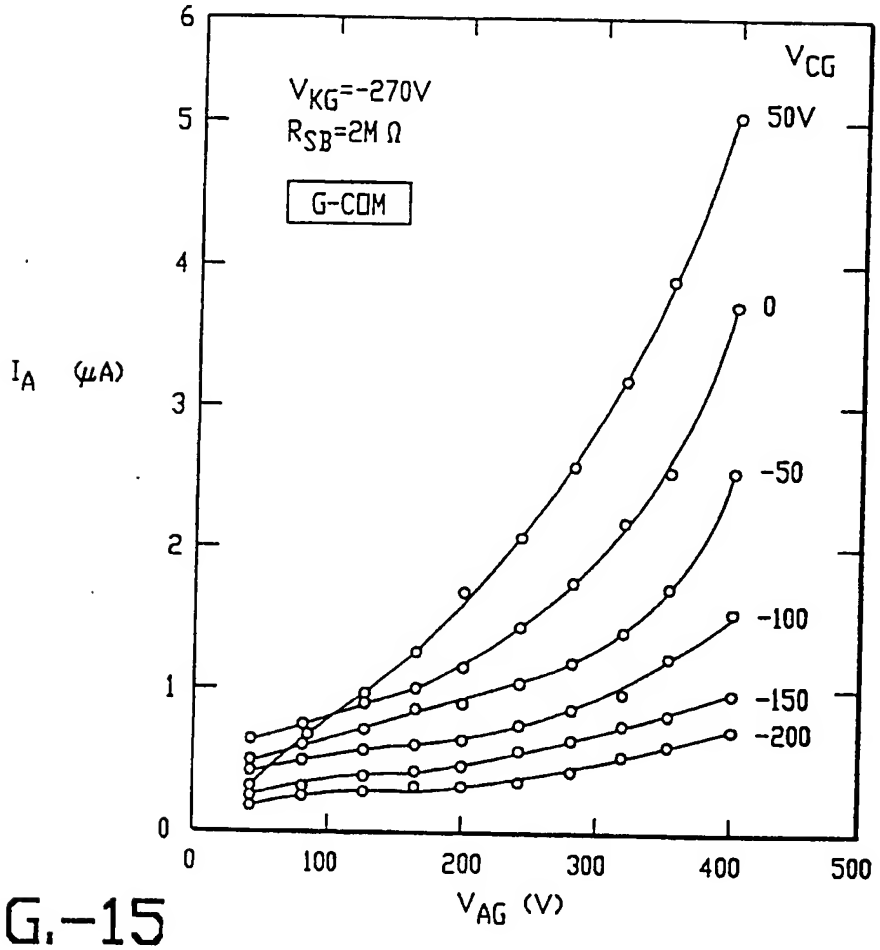

V_{CG}
V_{KG}=-270V
R_{SB}=2M Ω
G-COM
50V
0
-50
-100
-150
-200
I_A (μA)
V_{AG} (V)
0
1
2
3
4
5
6
100
200
300
400
500

FIG.-15

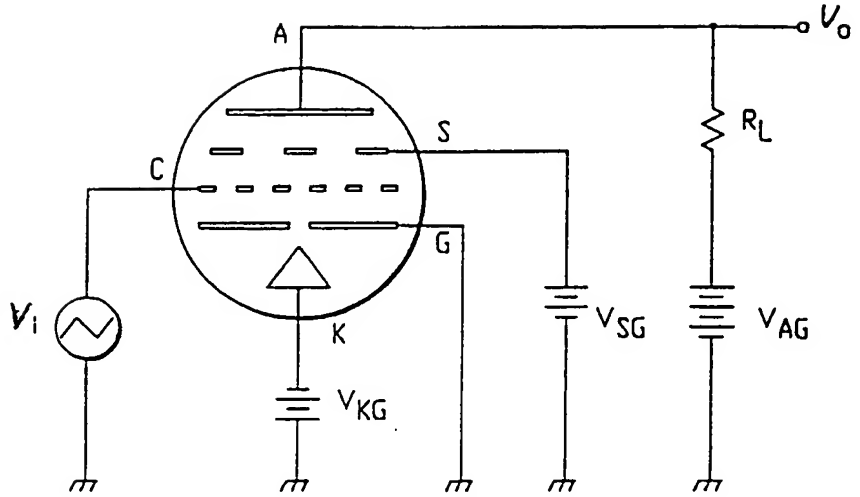

A
V_o
R_L
S
C
G
V_i
K
V_{SG}
V_{AG}
V_{KG}

FIG.-16

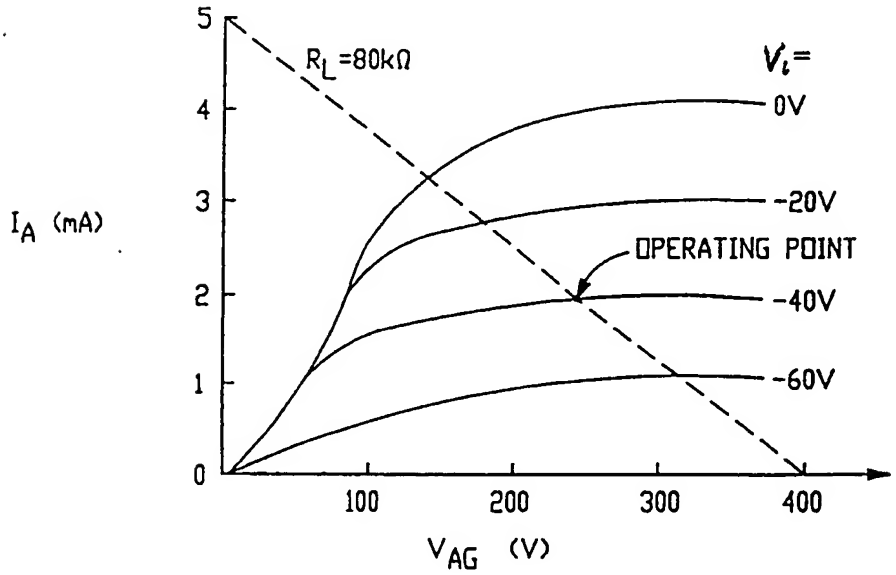

5
4
3
2
1
0
I_A (mA)
R_L=80kΩ
V_i=
0V
-20V
OPERATING POINT
-40V
-60V
100
200
300
400
V_{AG} (V)

FIG.-17

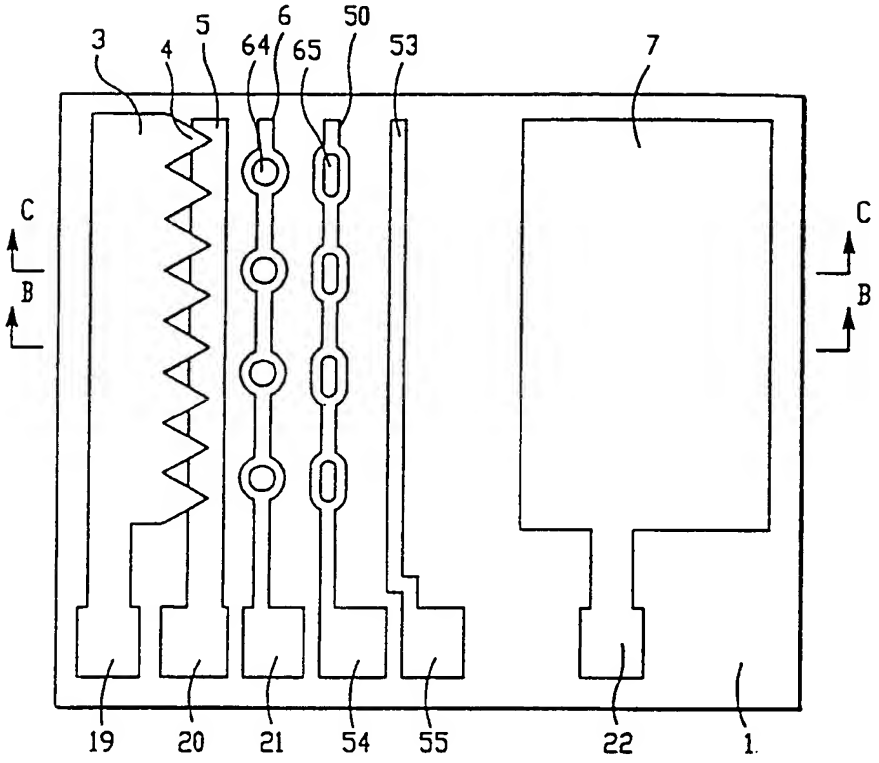


FIG.-18(A)

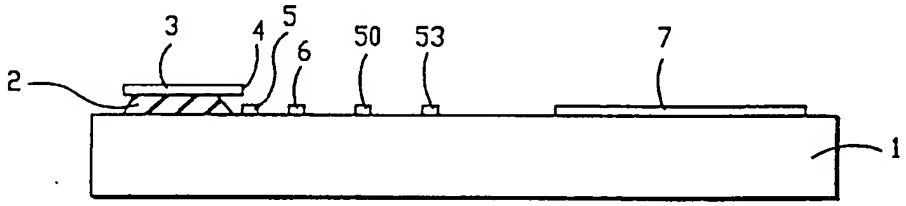


FIG.-18(B)

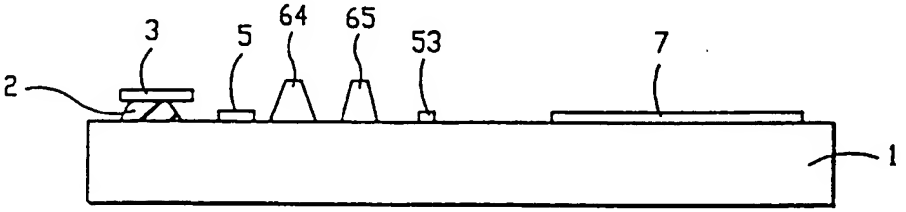


FIG.-18(C)

FIG.-19(A)

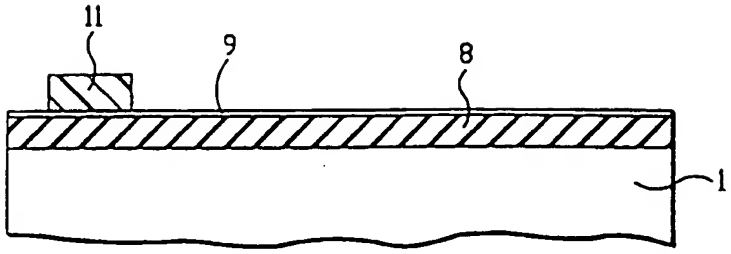


FIG.-19(B)

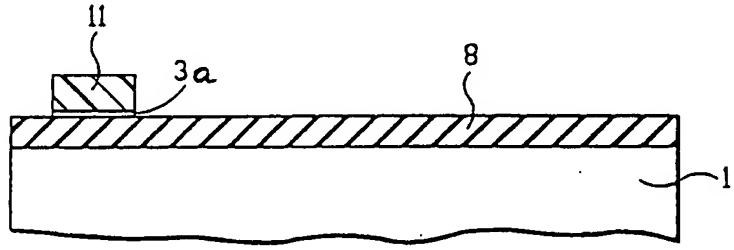


FIG.-19(C)

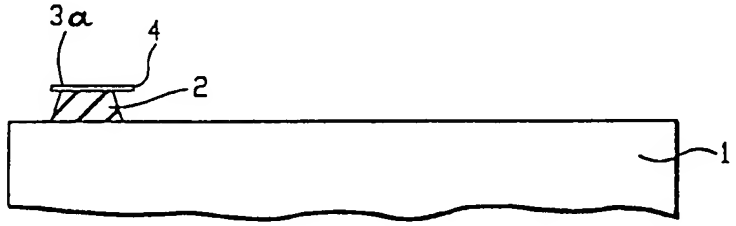


FIG.-19(D)

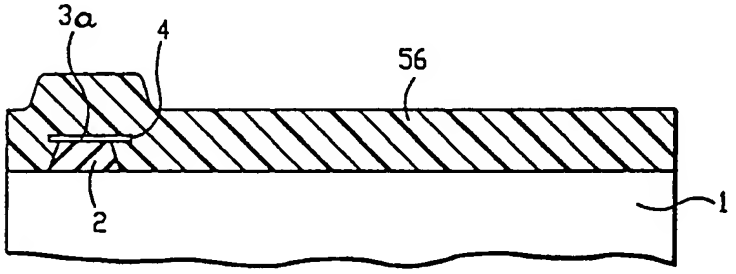
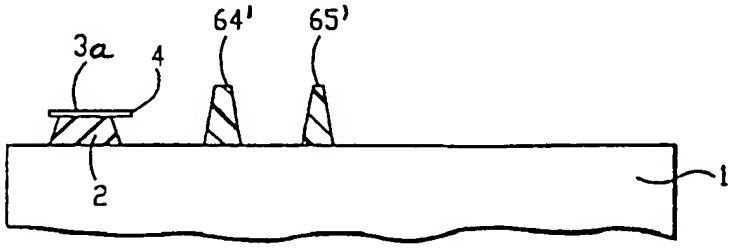


FIG.-19(E)



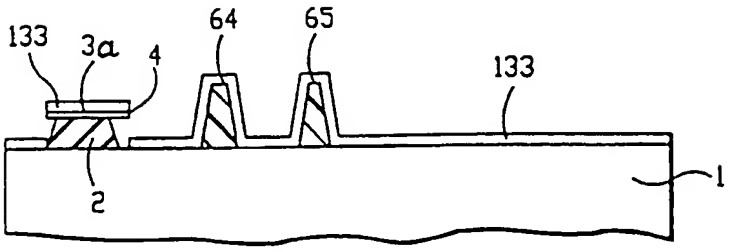


FIG.-19(F)

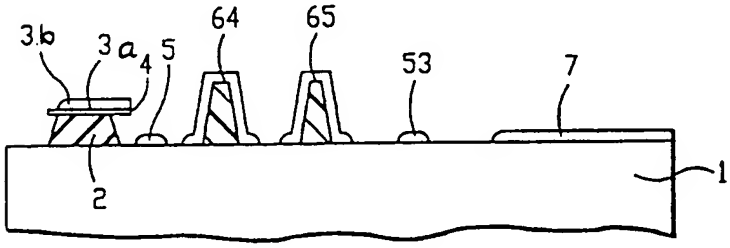


FIG.-19(G)

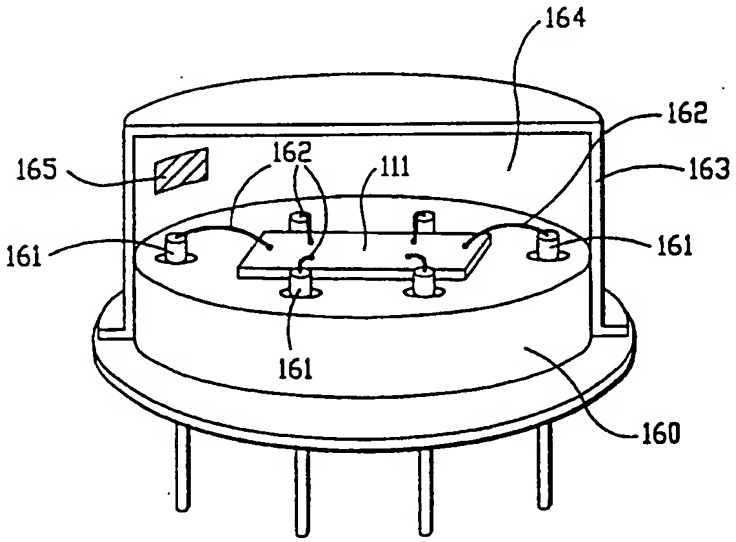


FIG.-20

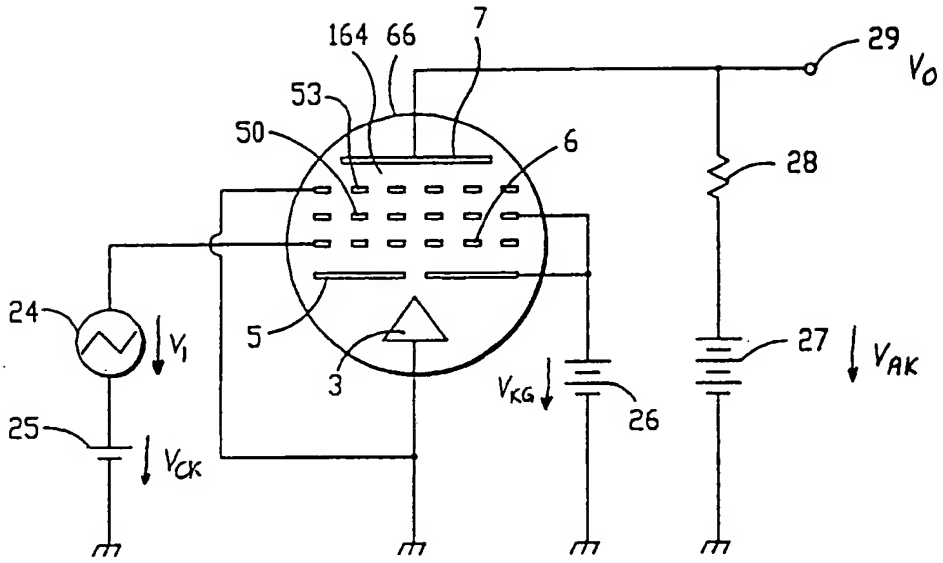

164
66
7
29
V_O
53
50
6
28
24
V_1
5
3
V_{KG}
26
27
V_{AK}
25
V_{CK}

FIG.-21

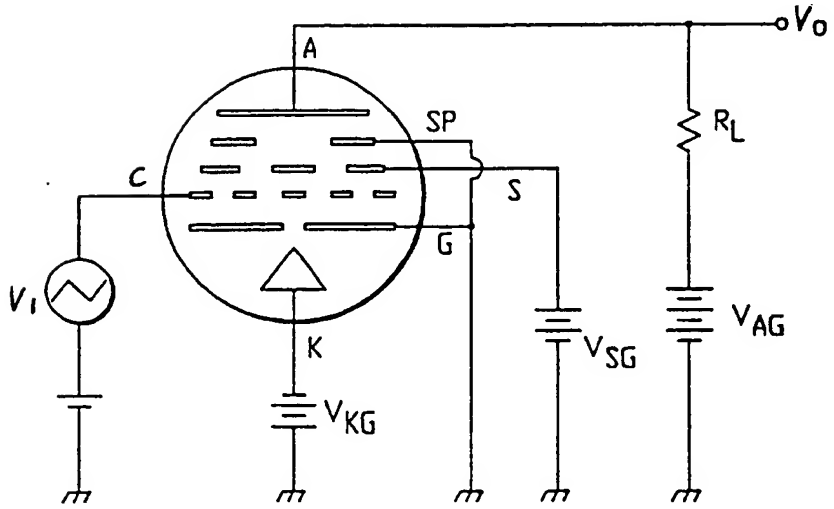

V_O
A
SP
R_L
C
S
G
V_1
K
V_{SG}
V_{AG}
V_{KG}

FIG.-22

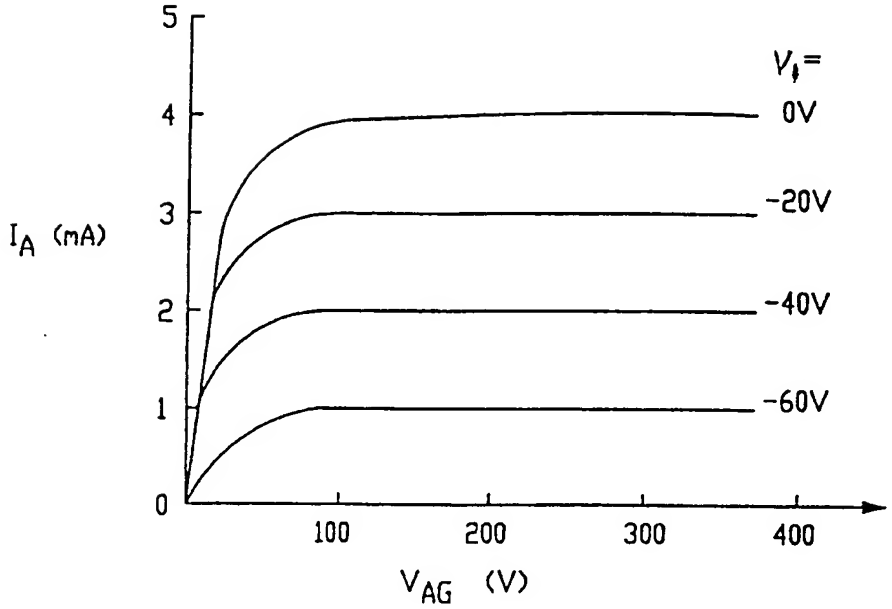

5
4
3
2
1
0
I_A (mA)
V_f =
0V
-20V
-40V
-60V
100
200
300
400
V_{AG} (V)

FIG.-23

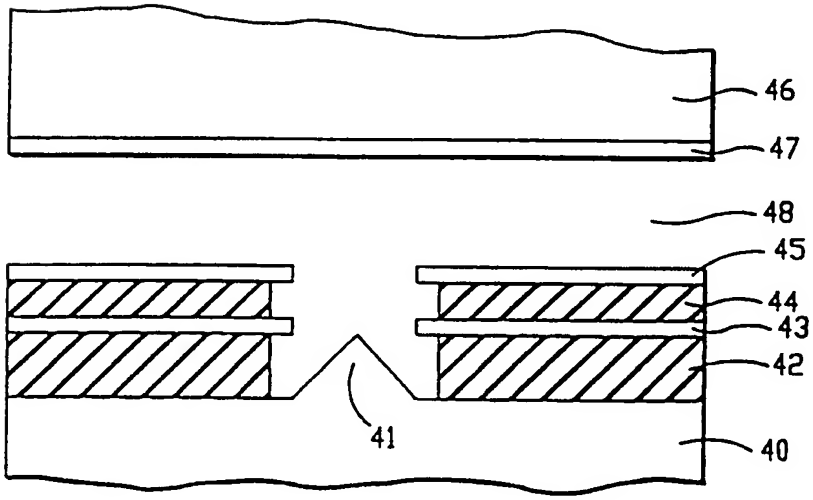

46
47
48
45
44
43
42
41
40

FIG.-24

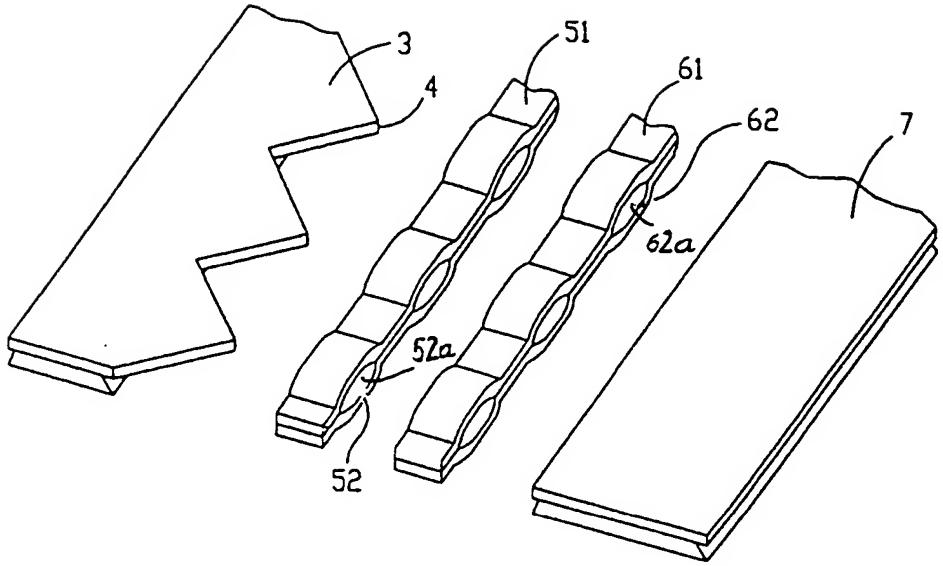


FIG.-25

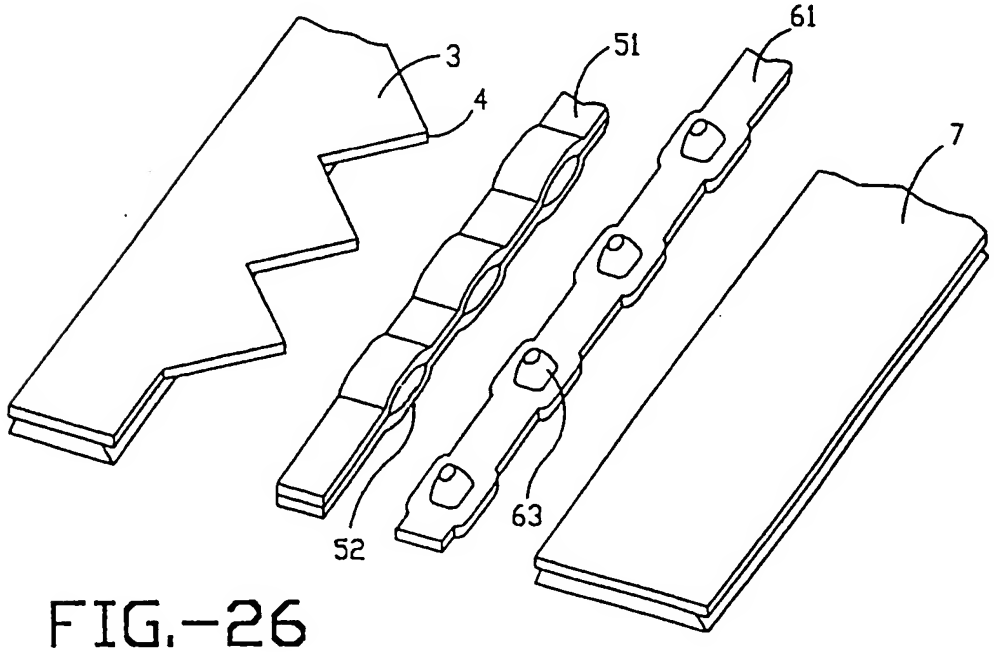


FIG.-26

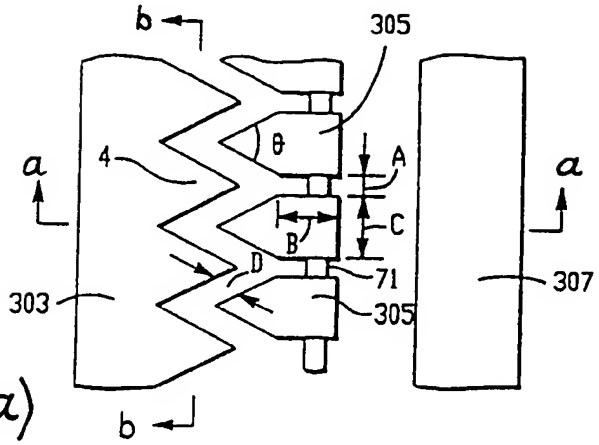


FIG.-27(a)

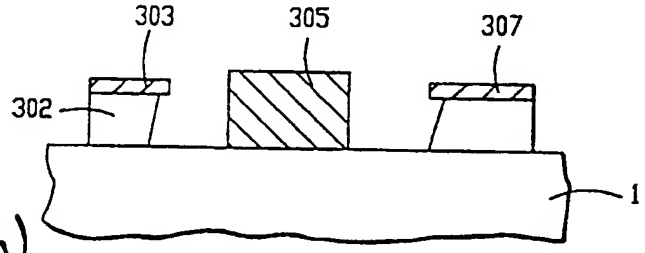


FIG.-27(b)

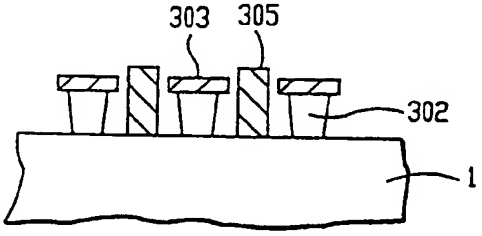


FIG.-27(c)

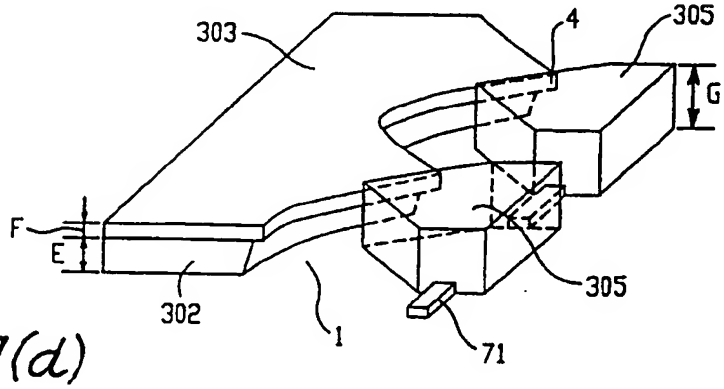


FIG.-27(d)

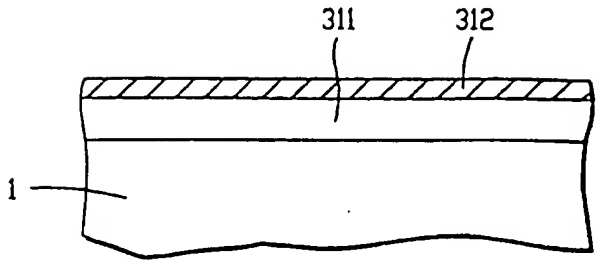


FIG.-28(a)

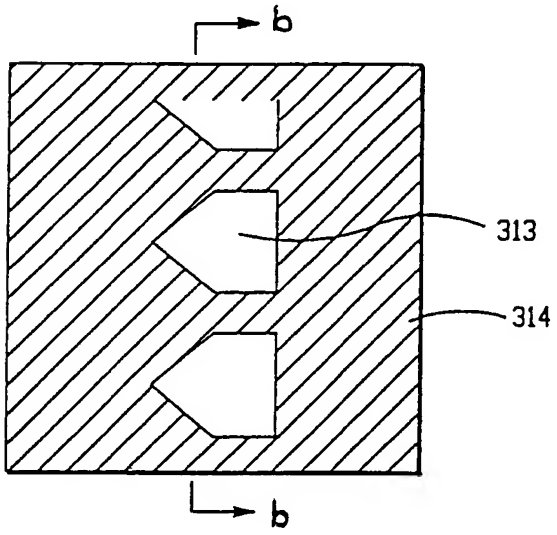


FIG.-28(b)

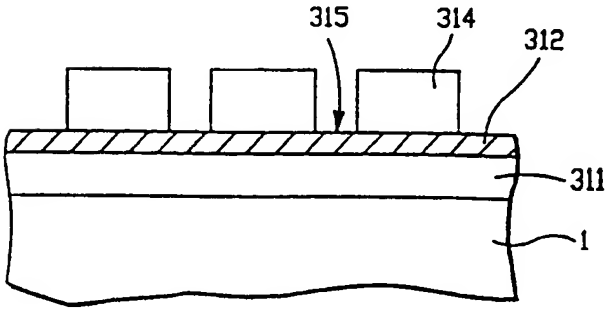


FIG.-28(c)

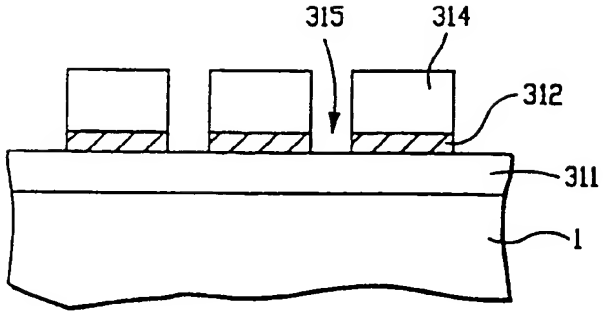


FIG.-29(a)

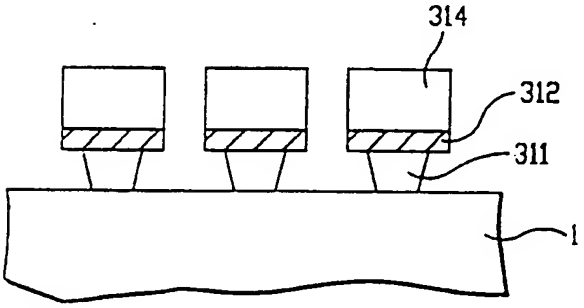


FIG.-29(b)

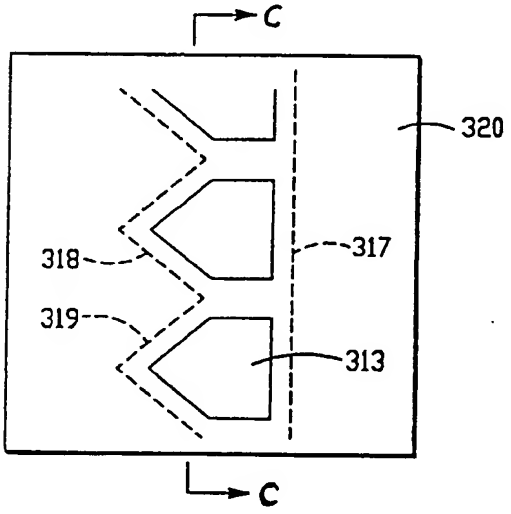


FIG.-29(c)

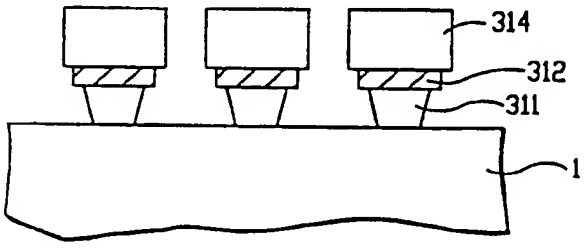


FIG.-29(d)

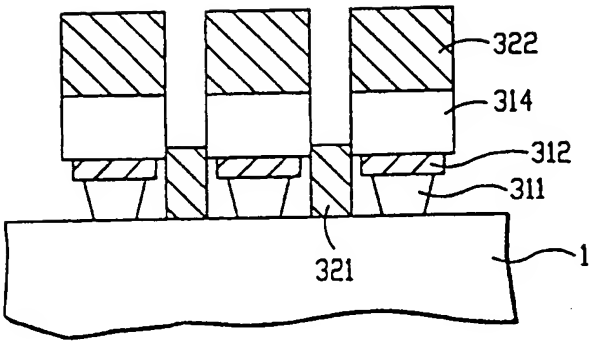


FIG.-30(a)

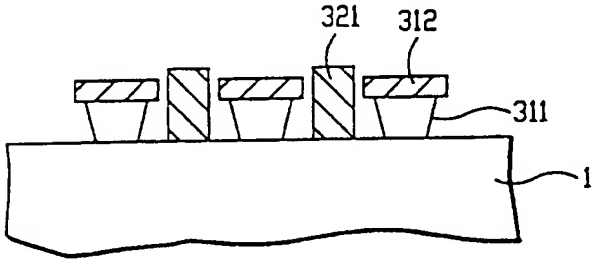


FIG.-30(b)

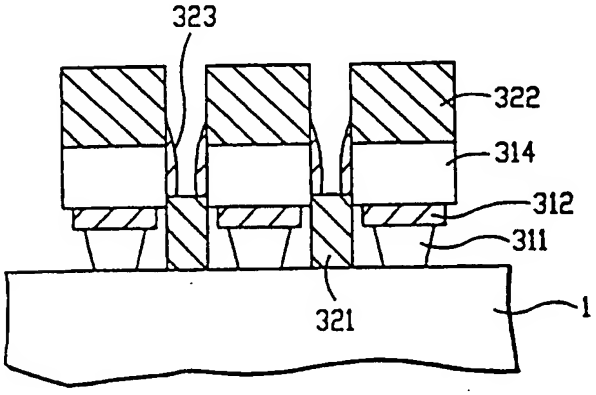


FIG.-31

FIG.-32(a)

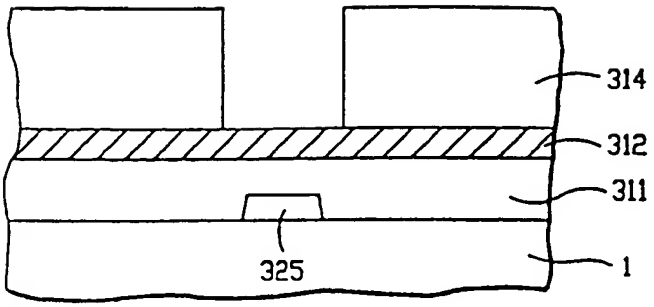


FIG.-32(b)

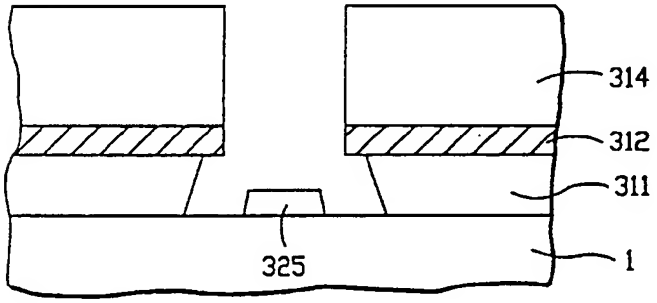


FIG.-32(c)

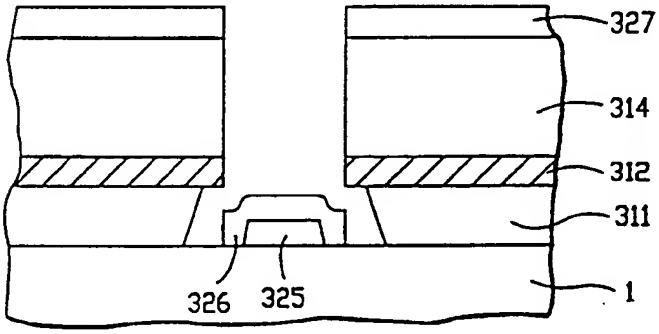


FIG.-32(d)

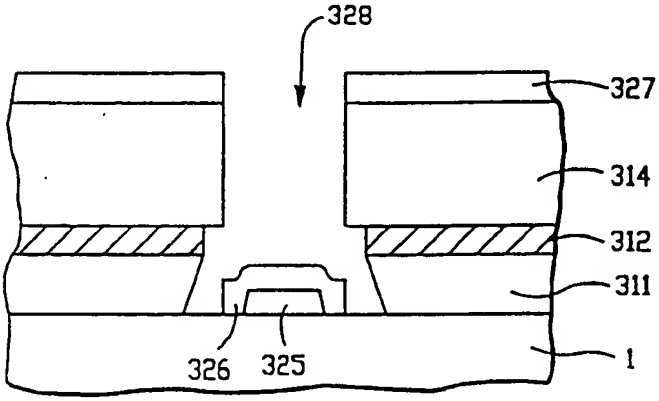


FIG.-32(e)

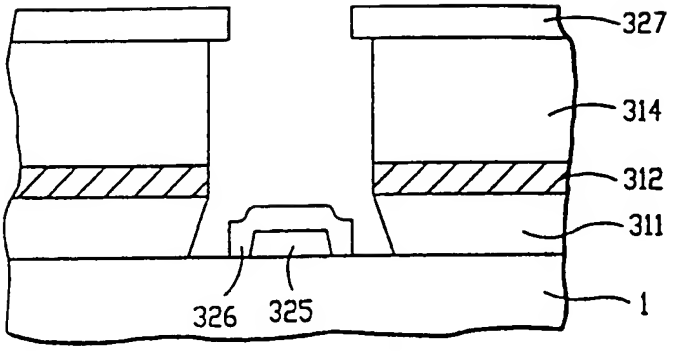


FIG.-32(f)

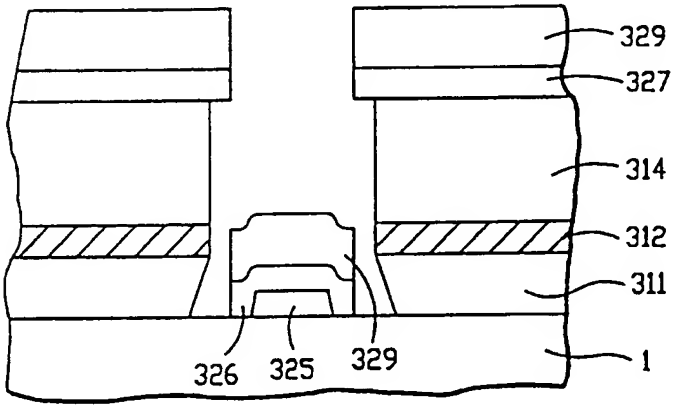
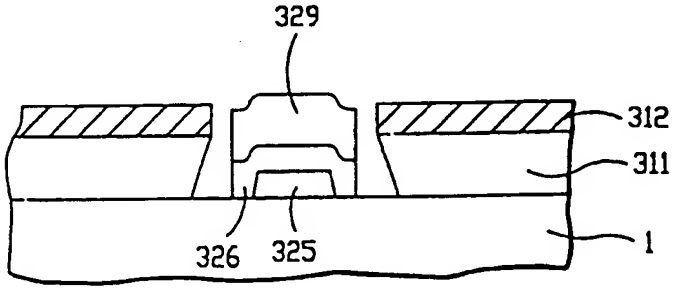


FIG.-32(g)



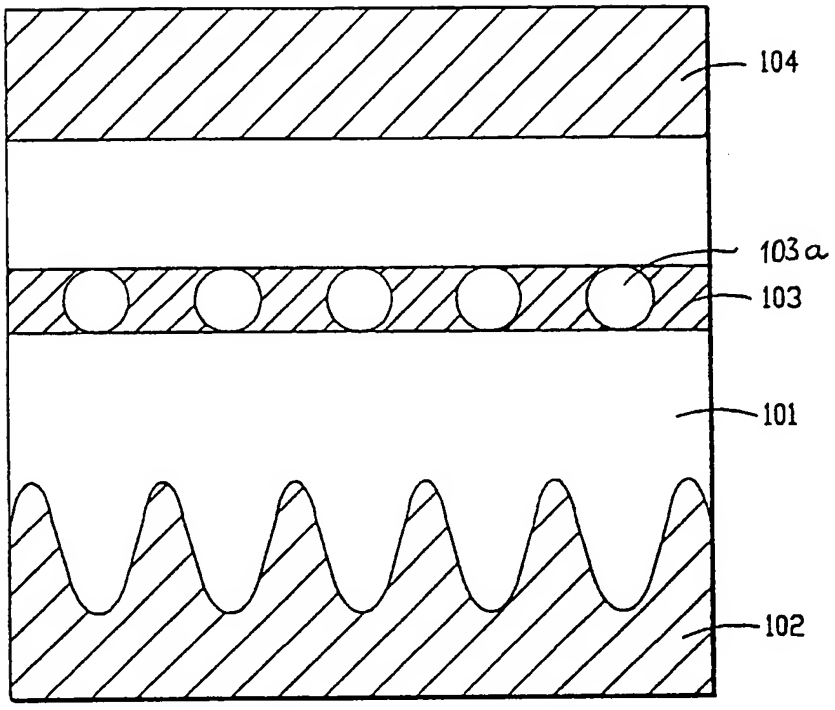


FIG.-33
PRIOR ART

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(54) Multiple electrode field electron emission device and process for manufacturing it.

(57) Disclosed is a multiple electrode field electron emission device having a cathode (3) for emitting electrons by means of the field effect, a gate electrode (5) for establishing an electric field between said cathode and said gate electrode, an anode (7) for collecting the emitted electrons, and a control electrode (6) placed between said cathode (3) and said anode (7) for controlling the emitted electrons. Disclosed is also a method for manufacturing such a device in a manner to achieve emission projections (4) of the cathode (3) with a very small curvature radius and perfectly aligned to the gate electrode (5).

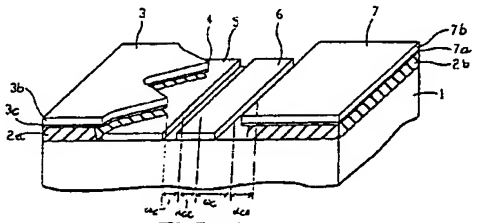

FIG.-1

EP 0 513 777 A3

European Patent Office

EUROPEAN SEARCH REPORT

Application Number EP 92108110.5

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
X	WO - A - 91/02 371 (MOTOROLU) * Page 2, line 29 - page 4, line 29; fig. 4 *	1	H 01 J 1/30 H 01 J 9/02
Y	* Page 2, line 29 - page 4, line 29; fig. 4 *	2,4, 10,11, 15,17	
X	US - A - 5 012 153 (ATKINSON) * Column 4, line 8 - column 6, line 10; fig. 2,4,6 *	1,9,20	
Y	* Column 4, line 8 - column 6, line 10; fig. 2,4,6 *	21,22	
A	* Column 4, line 8 - column 6, line 10; fig. 2,4,6 *	23,24	
X	EP - A - 0 376 825 (THOMSON) * Column 5, line 34 - column 9, line 27 *	1	TECHNICAL FIELDS SEARCHED (Int. Cl.5)
Y		2	H 01 J
A		3,5-8, 12	
X	PATENT ABSTRACTS OF JAPAN, unexamined application, section E, vol. 2, no. 153 December 22, 1978, THE PATENT OFFICE JAPANESE GOVERNMENT page 9826 E 78 * No. 53-121 454 (T.S.D.) *	1,9	
Y	EP - A - 0 406 886 (MATSUSHITA) * Column 6, lines 1-31;	4,10, 11,15, 17	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
VIENNA	11-08-1993	SCHLECHTER

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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EPO FORM 1503 03.82 (P0401)

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DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
	fig. 3 *		
A		16	
	--		
Y	EP - A - 0 444 670 (MATSUSHITA) * Column 3, line 49 - column 5, line 5 *	13,14	
A		18,19	
	--		
Y	EP - A - 0 400 406 (MATSUSHITA) * Column 10, line 47 - column 13, line 13 *	13,14	
	--		
Y	EP - A - 0 172 089 (COMMISSARIAT A L'ENERGIE ATOMIQUE) * Page 8, line 26 - page 10, line 27; fig. 3 *	21	
	--		
Y	EP - A - 0 316 214 (COMMISSARIAT A L'ENERGIE ATOMIQUE) * Column 6, lines 7-54; fig. 3 *	22	TECHNICAL FIELDS SEARCHED (Int. Cl.5)

The present search report has been drawn up for all claims

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